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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, FLYING_DUTCHMAN, MLB, K91F

REV B RELEASE, 01/31/11

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CPU DECOUPLING-I

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CPU DECOUPLING-II

K92_MLB

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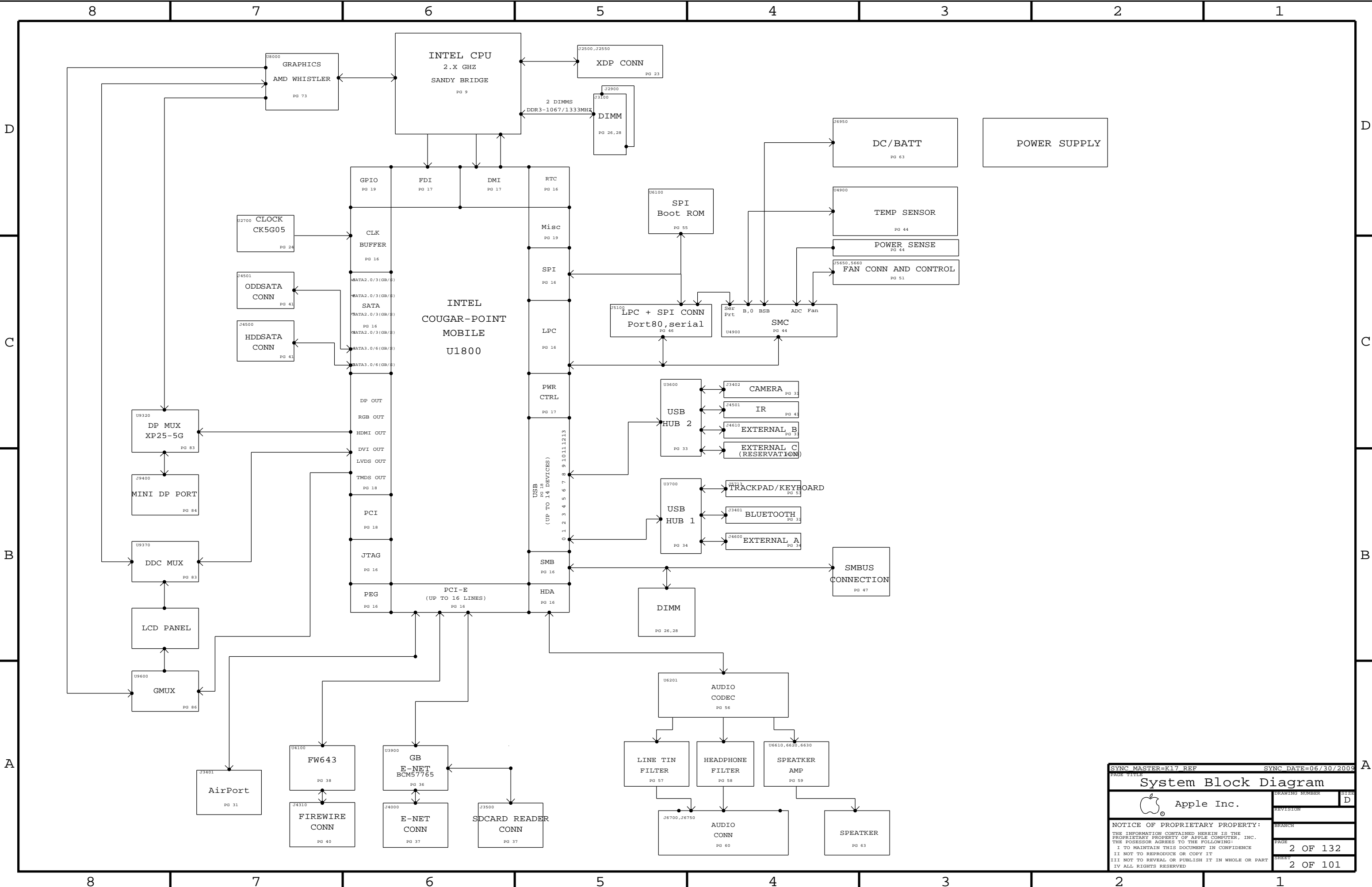
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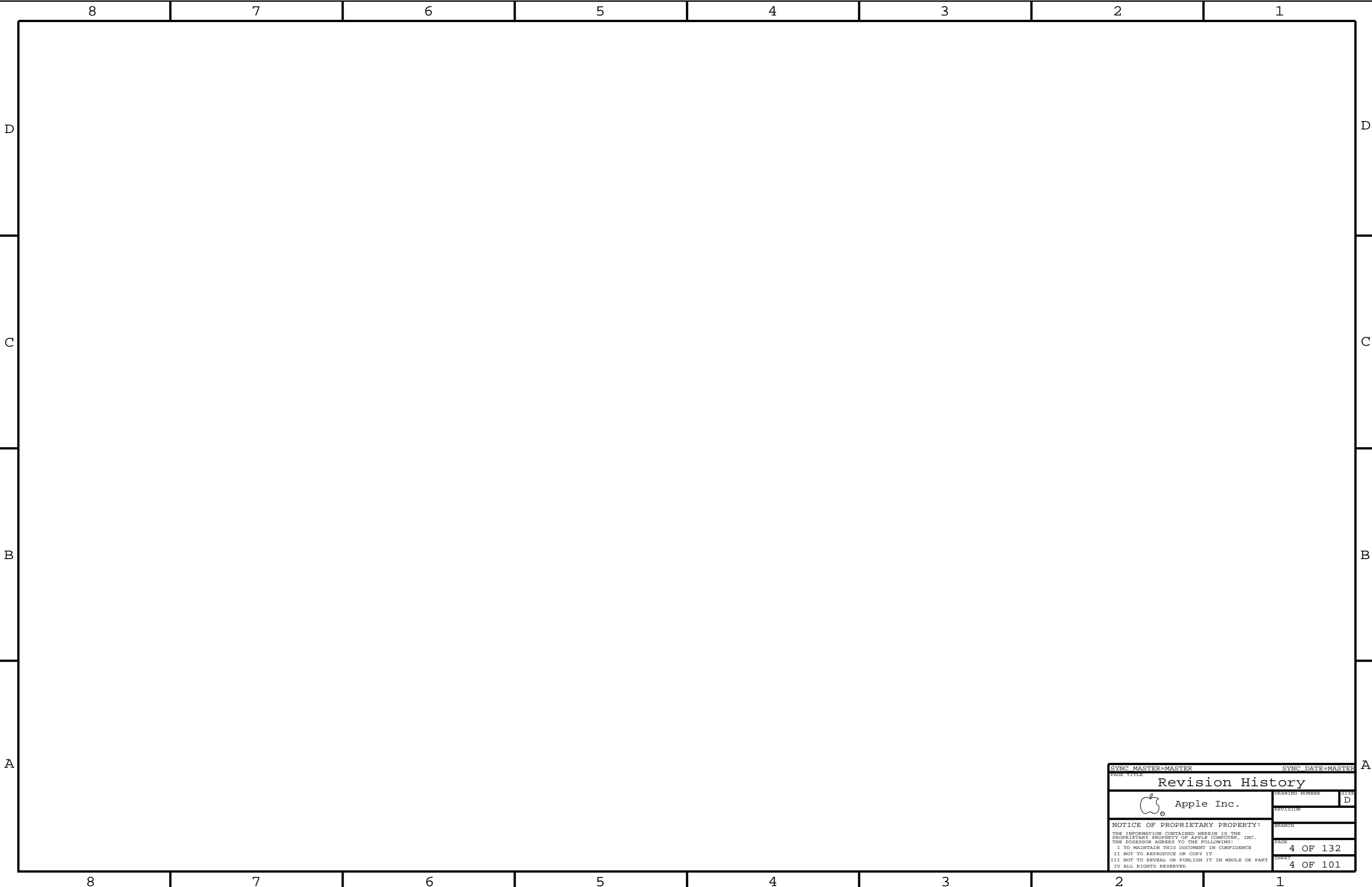
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SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
Revision History			
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		REVISION	D
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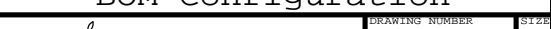
3

SMC

SYNC MASTER=K17 REF

SYNC MASTER=K17 REF SYNC DATE=05/28/2009

BOM Configuration



Apple Inc. D

REVISION

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REVISION

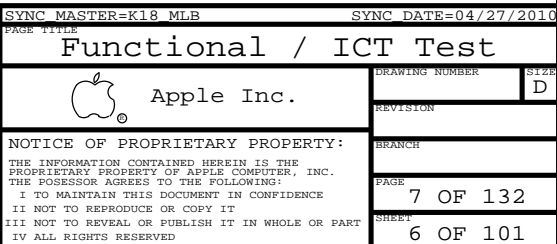
03/05/2012

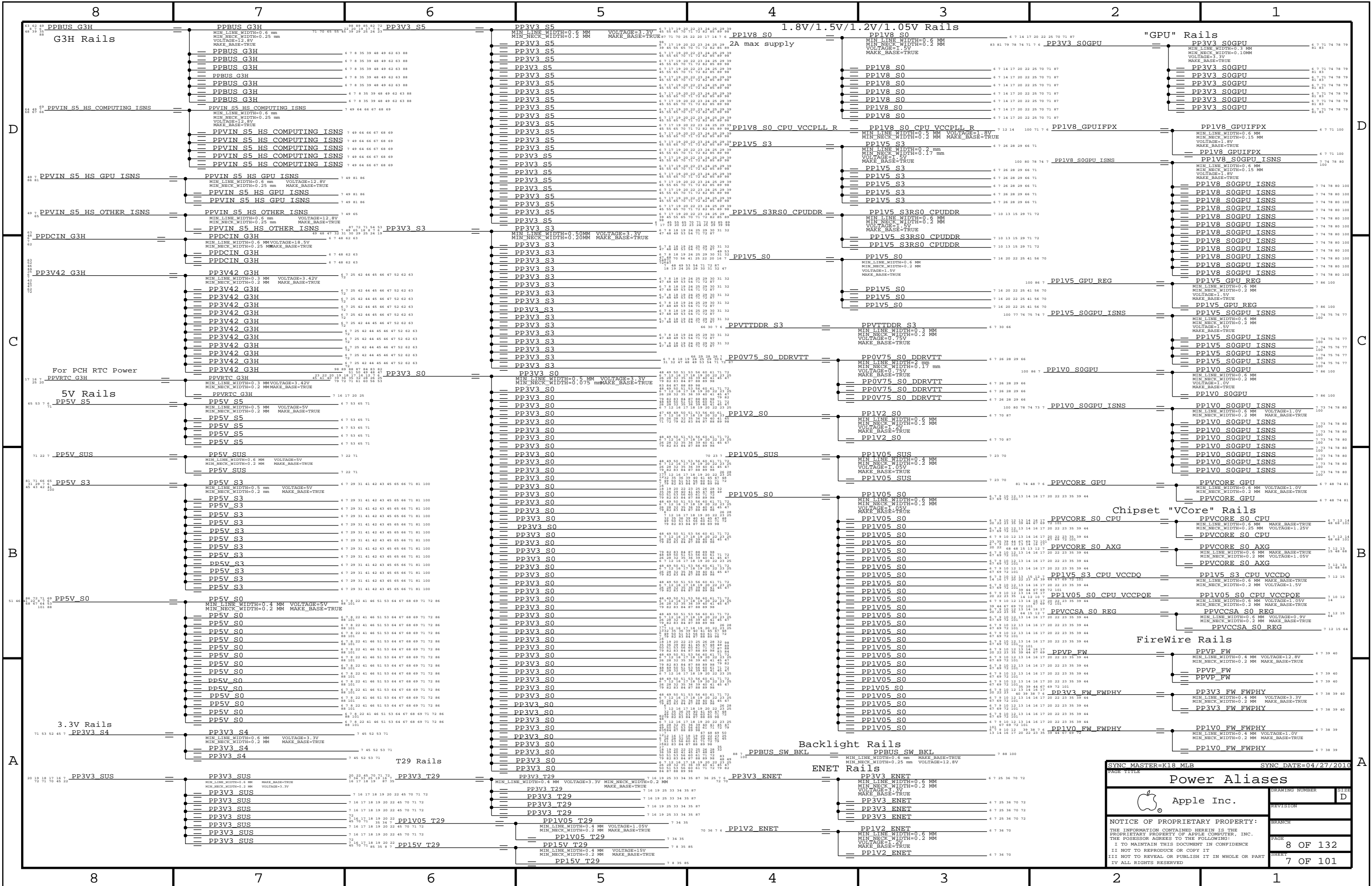
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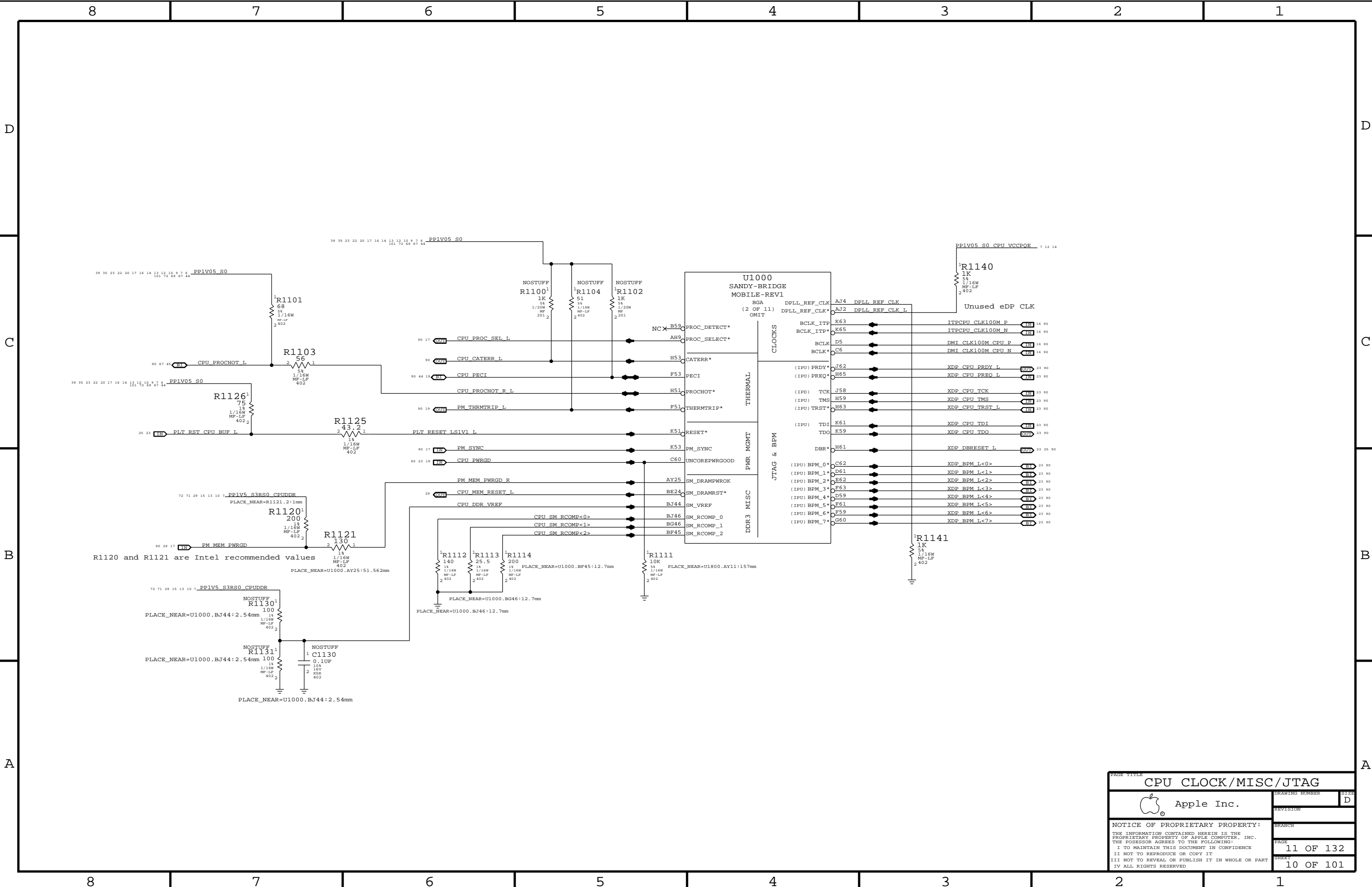
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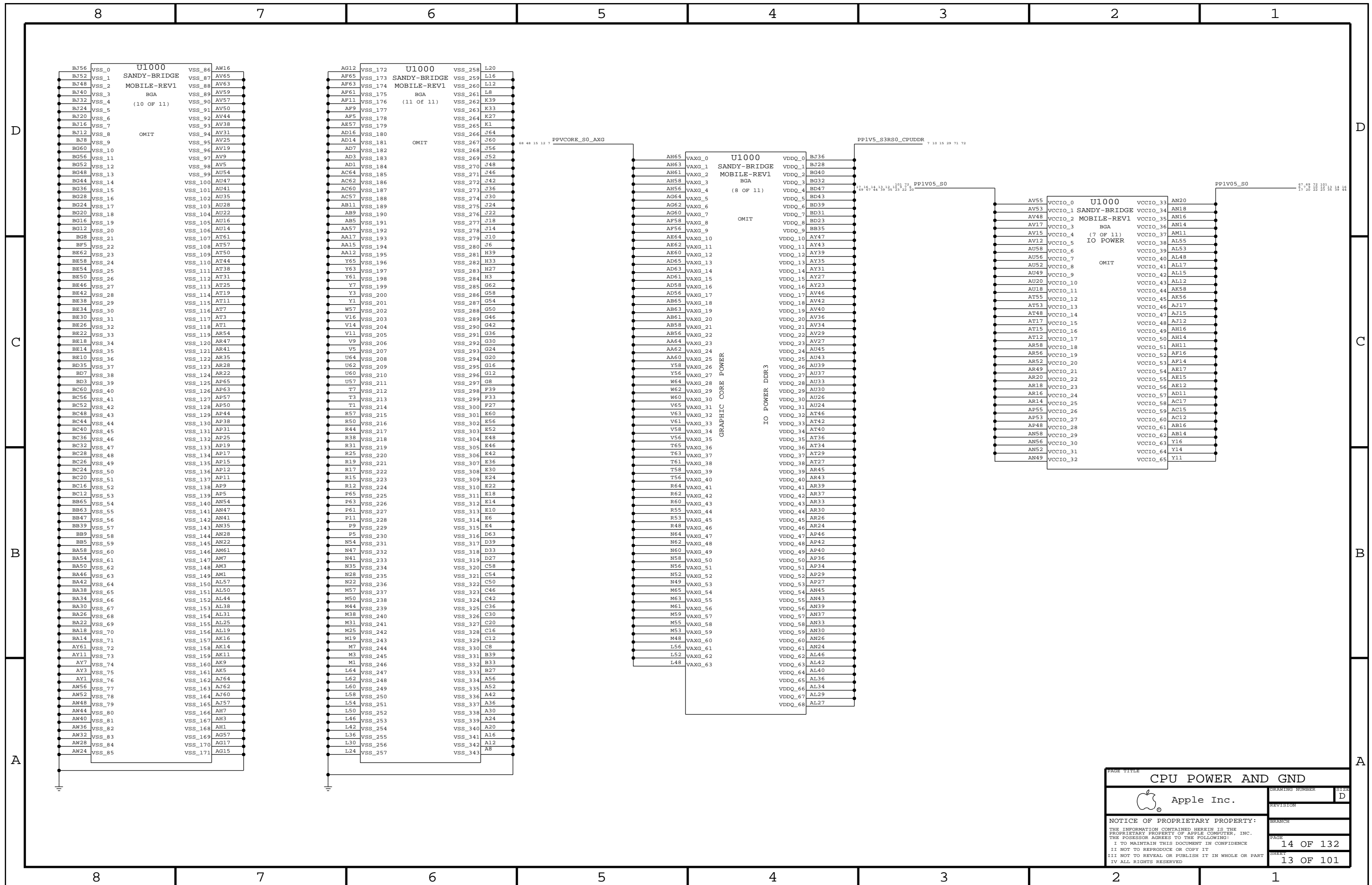
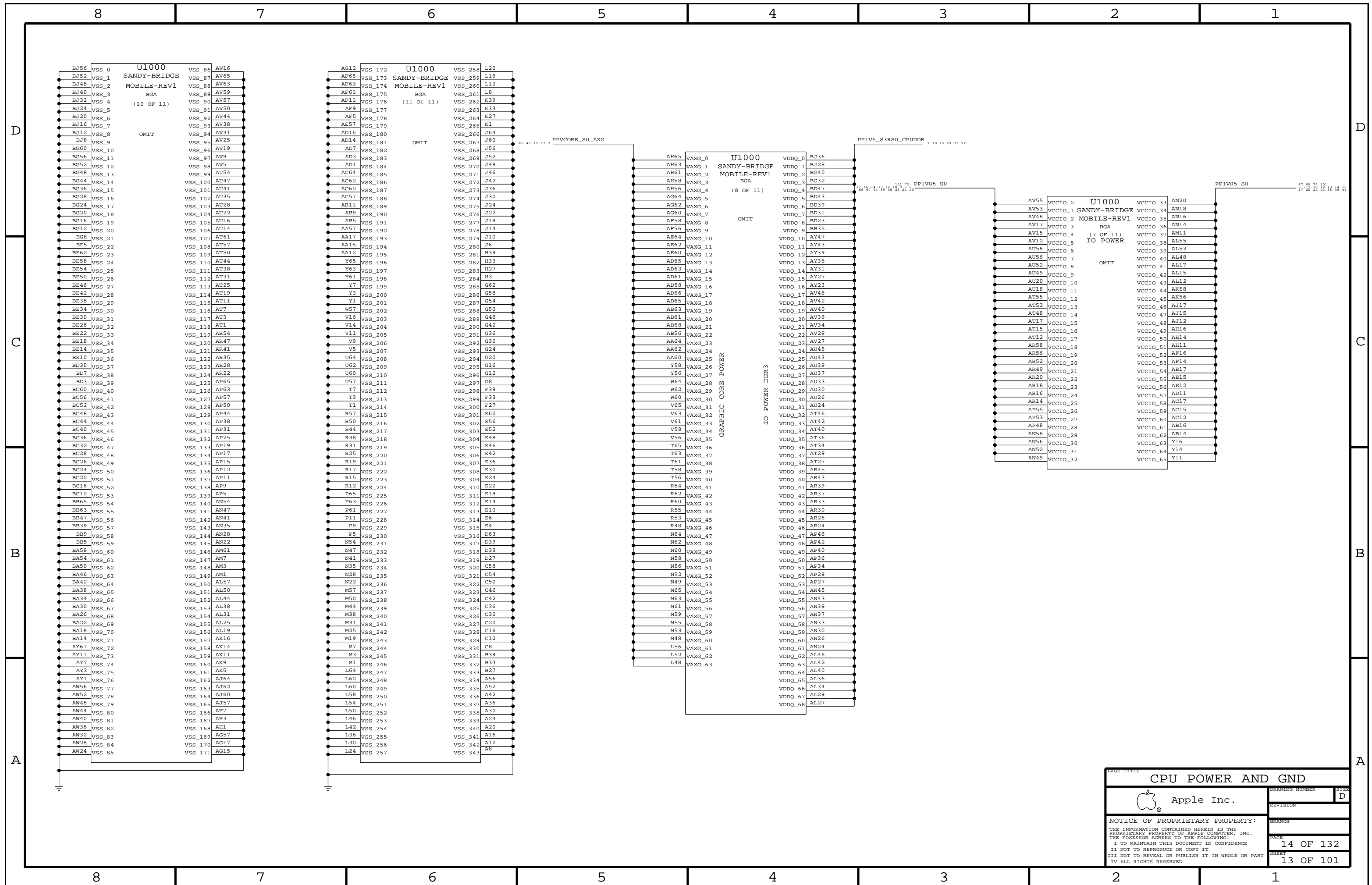






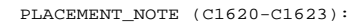


CPU DDR3 INTERFACES		DRAWING NUMBER	SIZE
Apple Inc.		REVISION	D
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Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

Place on bottom side of U1000



CRITICAL CRITICAL CRITICAL CRITICAL

C1620 C1621 C1622 C1623

1 1 1 1

10UF 10UF 10UF 10UF

20% 20% 20% 20%

6.3V 6.3V 6.3V 6.3V

CERM-X5R CERM-X5R CERM-X5R CERM-X5R

0402-1 0402-1 0402-1 0402-1

2 2 2 2

Place near Inductors on bottom side.

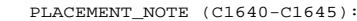
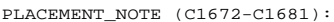


Figure 1: Schematic diagram of the test circuit. The circuit consists of five parallel branches connected to a common ground. The first four branches are labeled "CRITICAL" and each contains a 16440, 1641, 1642, and 1643 component respectively, all with a 470UF-4MOHM capacitor and a 20S resistor. The fifth branch is labeled "NOSTUFF" and contains a 1644 component with a 470UF-4MOHM capacitor and a 20S resistor. Each component is connected to a 2.0V POLY-TANT D2T-SM source.

Intel recommendation:	2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation:	2x 330uF, 10x 10uF 0603, 26x 1uF 0402

Place on bottom side of U1000



1 CRITICAL 1 CRITICAL 1 CRITICAL 1 CRITICAL 1 CRITICAL 1 CRITICAL 1 CRITICAL 1 CRITICAL 1 CRITICAL 1 CRITICAL

1 C1672 1 C1673 1 C1674 1 C1675 1 C1676 1 C1677 1 C1678 1 C1679 1 C1680 1 C1681

10UF 10UF 10UF 10UF 10UF 10UF 10UF 10UF 10UF 10UF 10UF

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6.3V 6.3V 6.3V 6.3V 6.3V 6.3V 6.3V 6.3V 6.3V 6.3V 6.3V

X5R X5R X5R X5R X5R X5R X5R X5R X5R X5R X5R

603 603 603 603 603 603 603 603 603 603 603

1 C1682 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

1 CRITICAL C1683 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

R1601
0.010
1 2
1/4W
MF
0603

PP1V05 **80** **CPU VCCPQE** 7 10 12

C1684
1 1uF
10V
2 XSR
402

Diagram illustrating the CPU VCCPLL Low pass filter circuit. The circuit includes a resistor R1600 (1.6M) and three capacitors: C1685 (1uF), C1686 (1uF), and C1687 (330uF). The output is connected to the PE1VR_S0_CPU_VCCPLL_R pin (pin 7). The diagram also shows the placement coordinates for the components.

Component values and labels:


- R1600: 1.6M
- C1685: 1uF
- C1686: 1uF
- C1687: 330uF

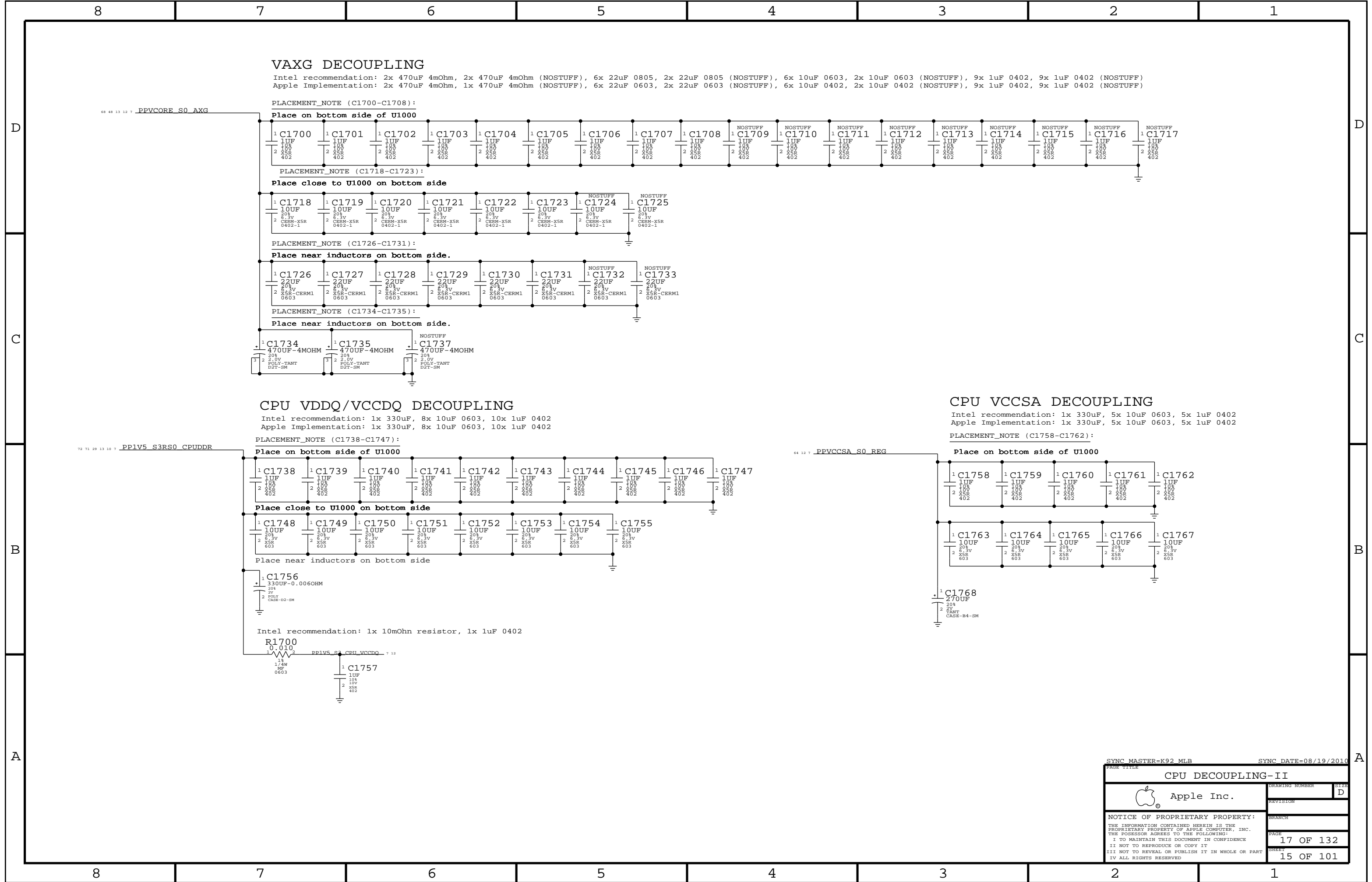
Pin labels and coordinates:

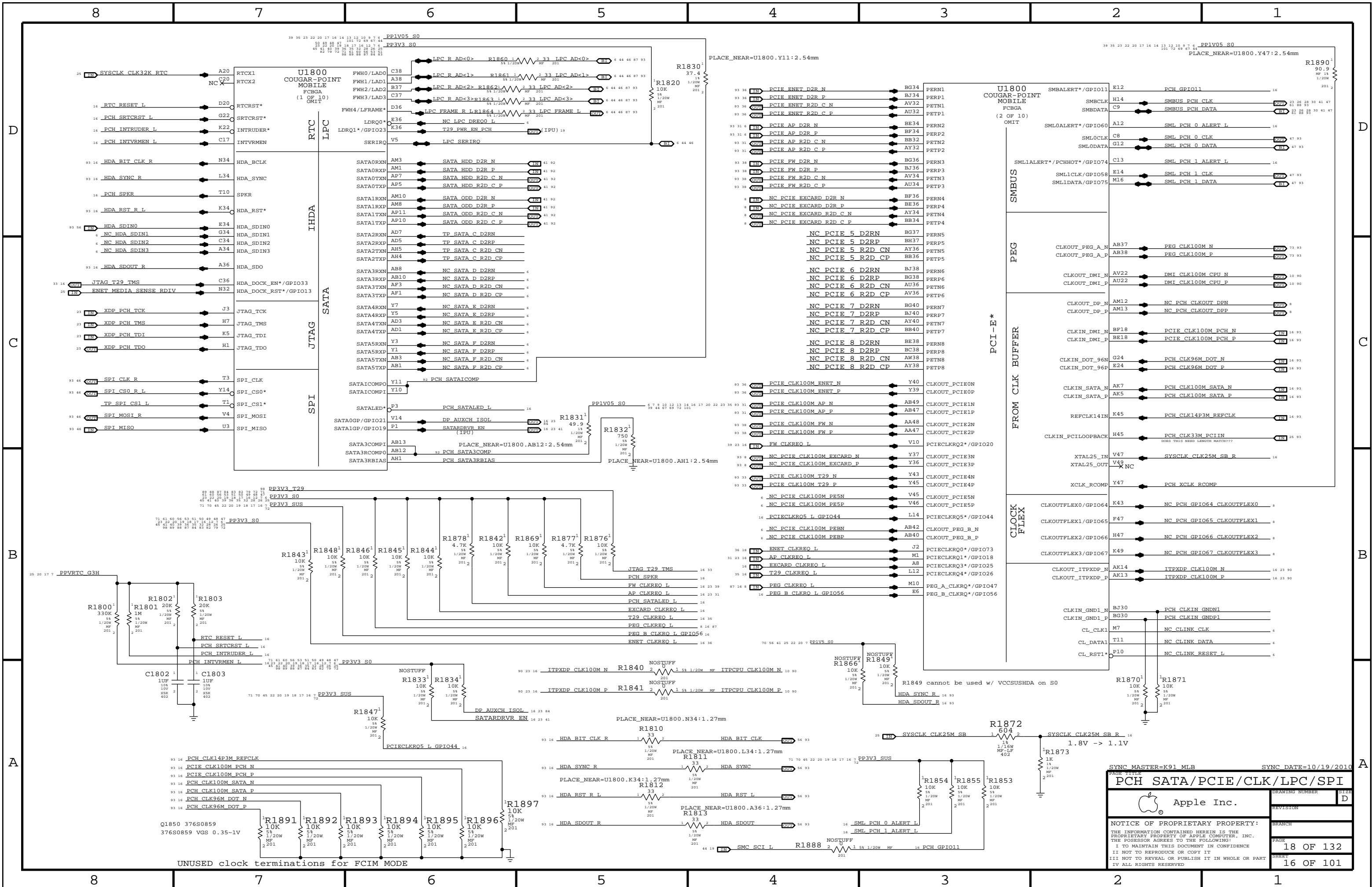
- Pin 1: PLACE_NEAR=U1000.AK612.54 mm; NO_VIA
- Pin 2: PLACE_NEAR=U1000.AK6512.54 mm; NO_VIA
- Pin 7: PE1VR_S0_CPU_VCCPLL_R

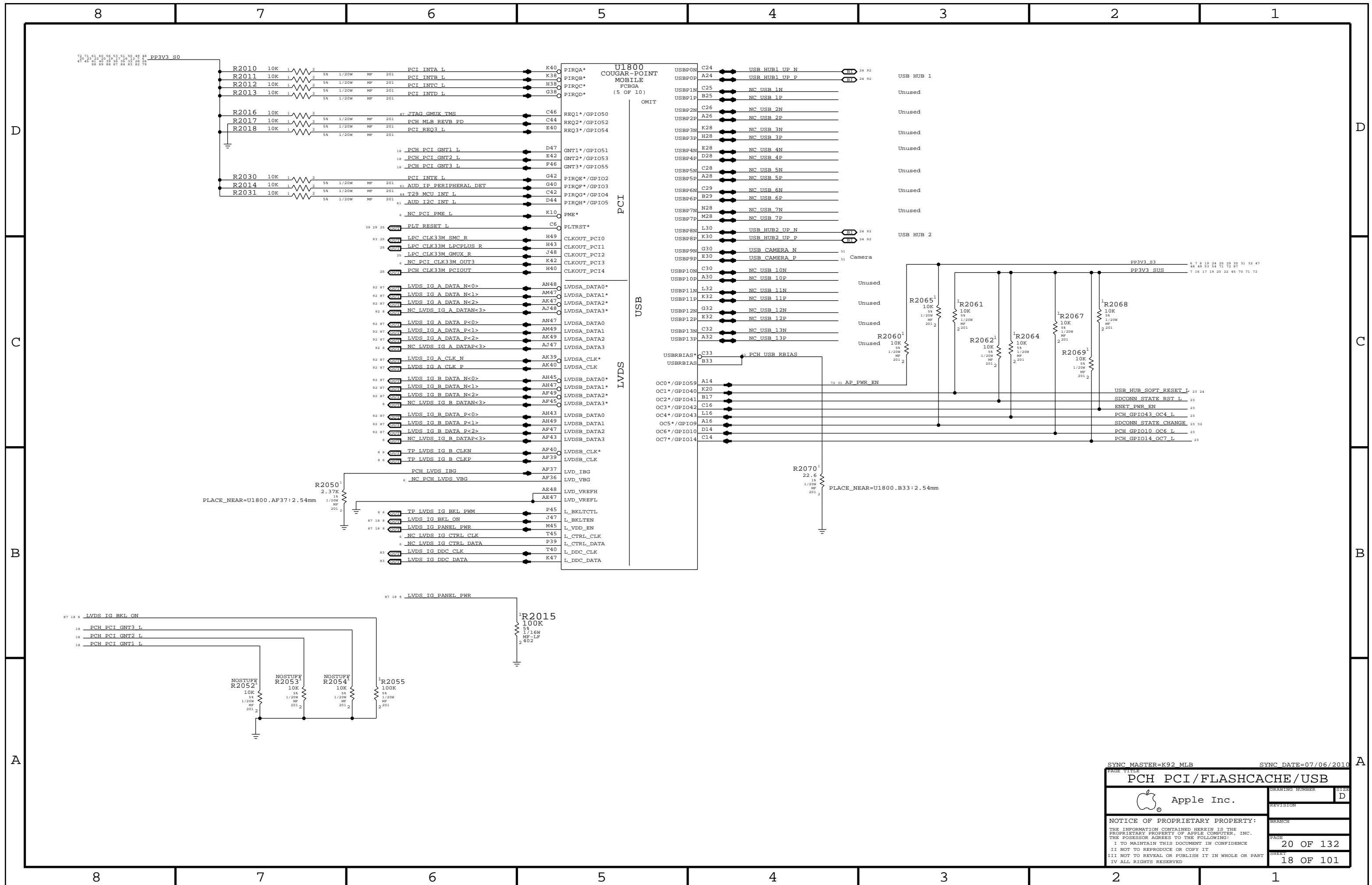
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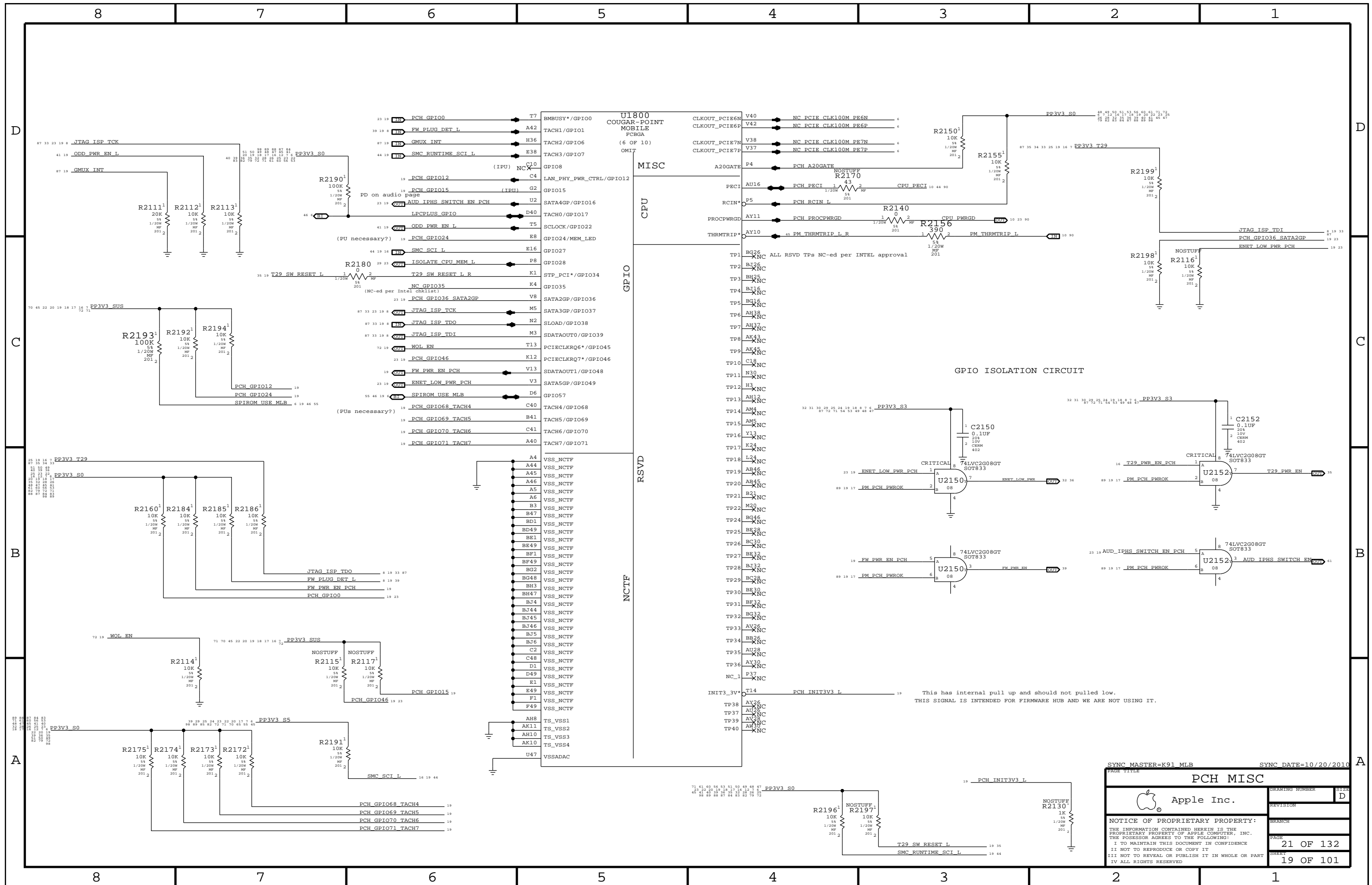
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- PLACE_NEAR=U1000.AK612.54 mm; NO_VIA

SYNC MASTER=K92 MLB		SYNC DATE=08/19/2010	
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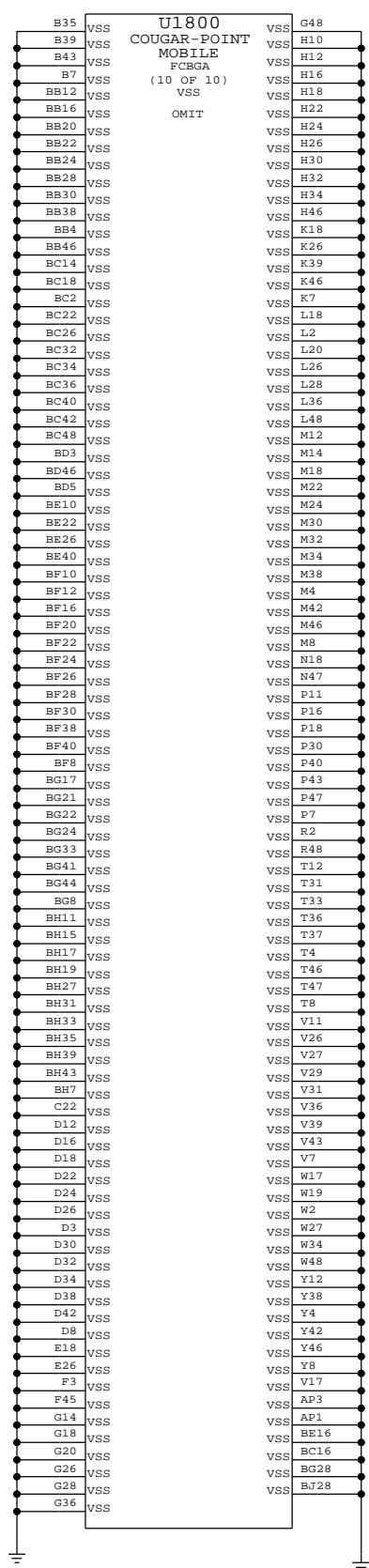
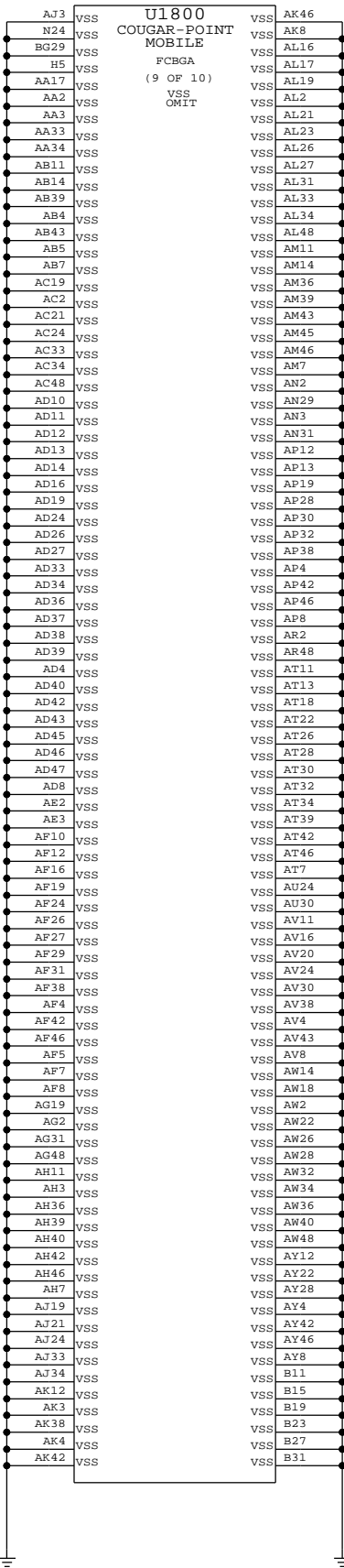
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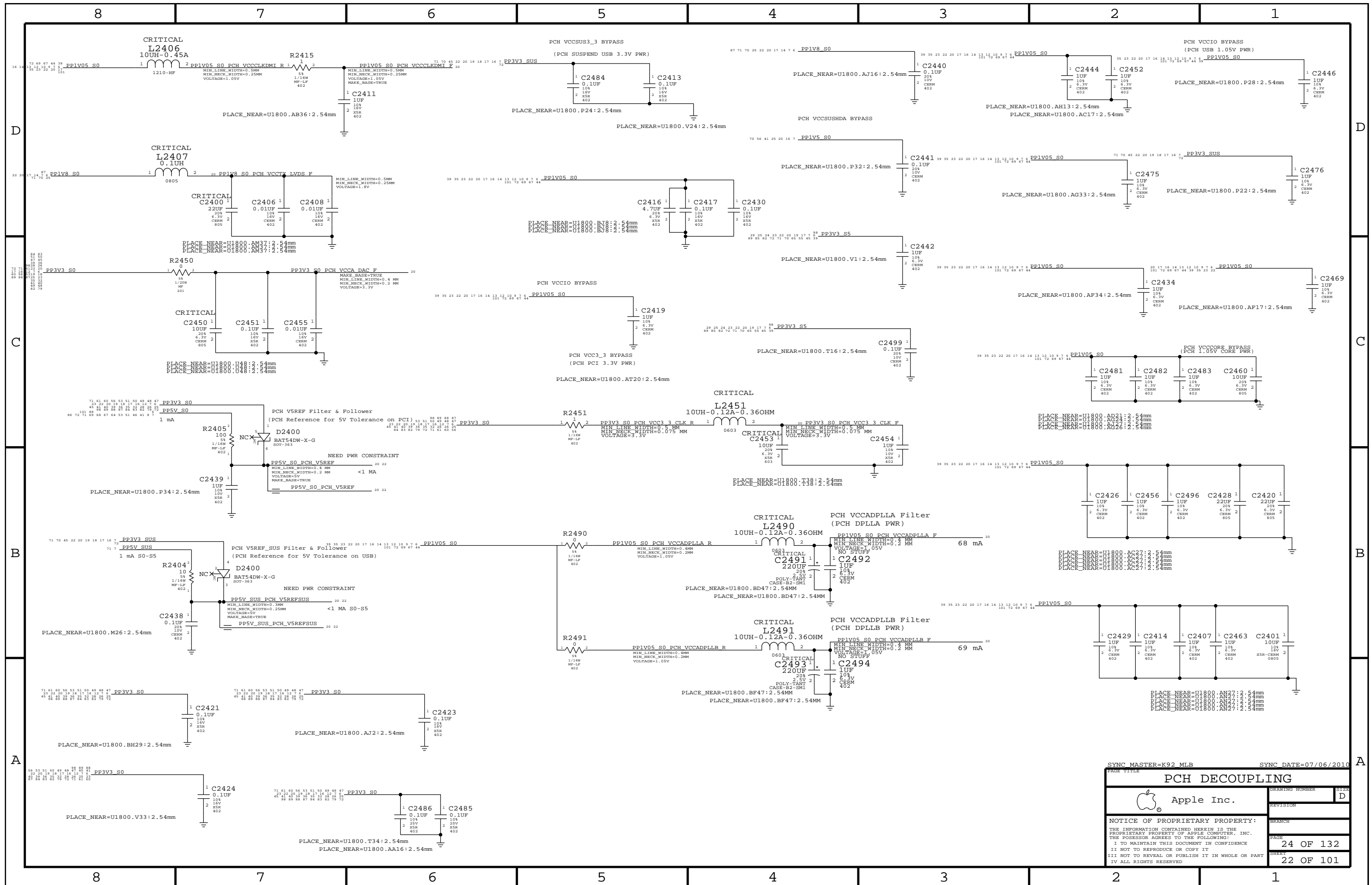
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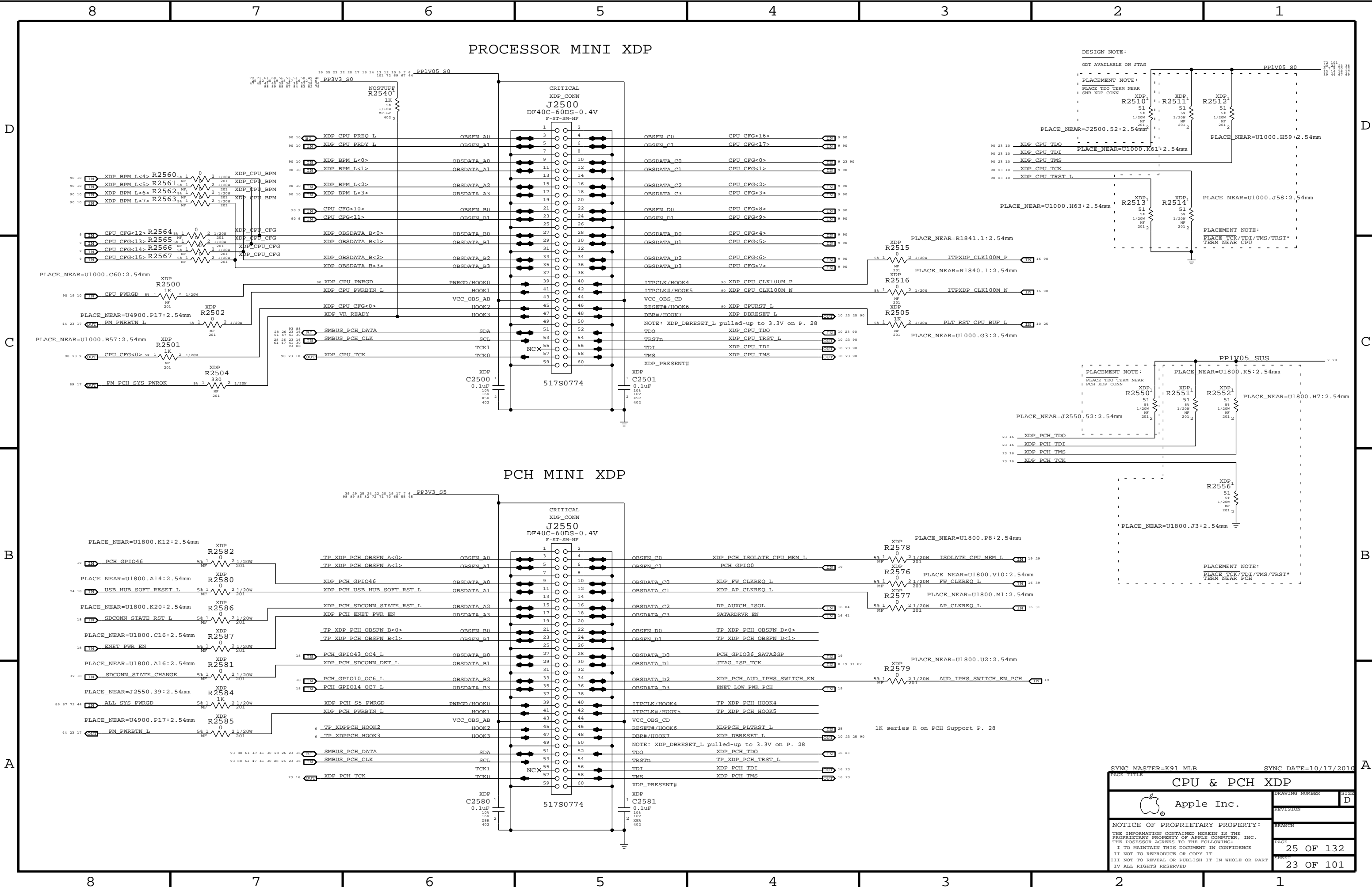


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SYNC DATE=04/30/2010

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DESIGN NOTE:
ODT AVAILABLE ON JTAG

PLACEMENT NOTE:
PLACE TDO TERM NEAR
SNB XDP CONN

PLACE_NEAR=J2500.52:2.54mm
PLACE_NEAR=U1000.K61:2.54mm
PLACE_NEAR=U1000.H59:2.54mm

PLACE_NEAR=U1000.H63:2.54mm
PLACE_NEAR=U1000.J58:2.54mm

PLACE_NEAR=U1000.G3:2.54mm
PLACE_NEAR=U1000.H7:2.54mm

PLACE_NEAR=U1000.H7:2.54mm
PLACE_NEAR=U1800.H7:2.54mm

PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.H7:2.54mm

PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.H7:2.54mm

PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.H7:2.54mm

PLACE_NEAR=U1800.H7:2.54mm
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PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.H7:2.54mm

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PLACE_NEAR=U1800.H7:2.54mm

PLACE_NEAR=U1800.H7:2.54mm
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PLACE_NEAR=U1800.H7:2.54mm
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PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.H7:2.54mm

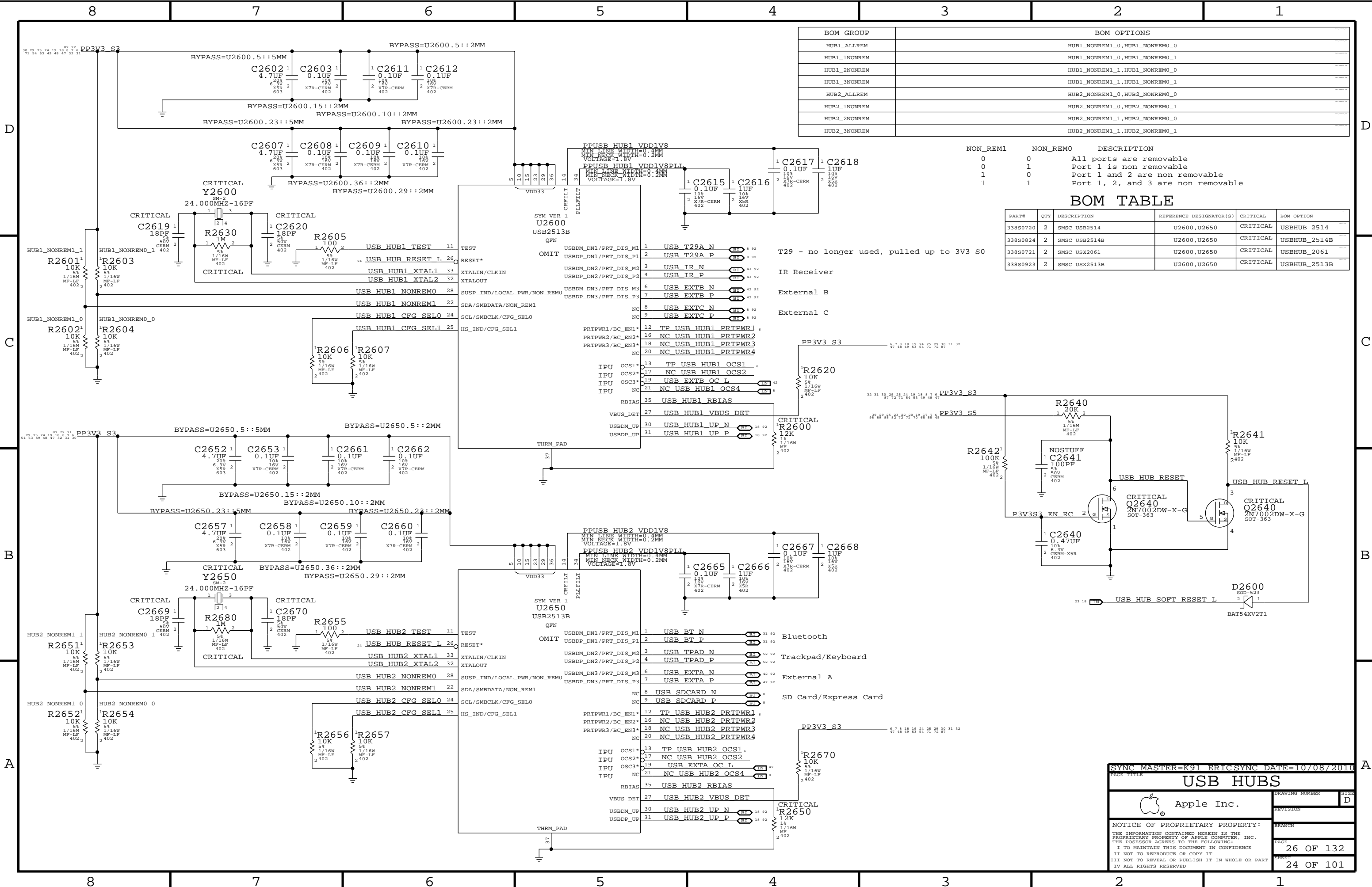
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PLACE_NEAR=U1800.H7:2.54mm

PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.H7:2.54mm

PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.H7:2.54mm

PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.H7:2.54mm

PAGE TITLE		SYNC DATE=10/17/2010	
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Apple Inc.		SIZE D	
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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0, HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0, HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1, HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1, HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0, HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0, HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1, HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1, HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600, U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600, U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600, U2650	CRITICAL	USBHUB_2061
338S0923	2	SMSC USX2513B	U2600, U2650	CRITICAL	USBHUB_2513B

T29 - no longer used, pulled up to 3V3 S0

IR Receiver

External B

External C

Bluetooth

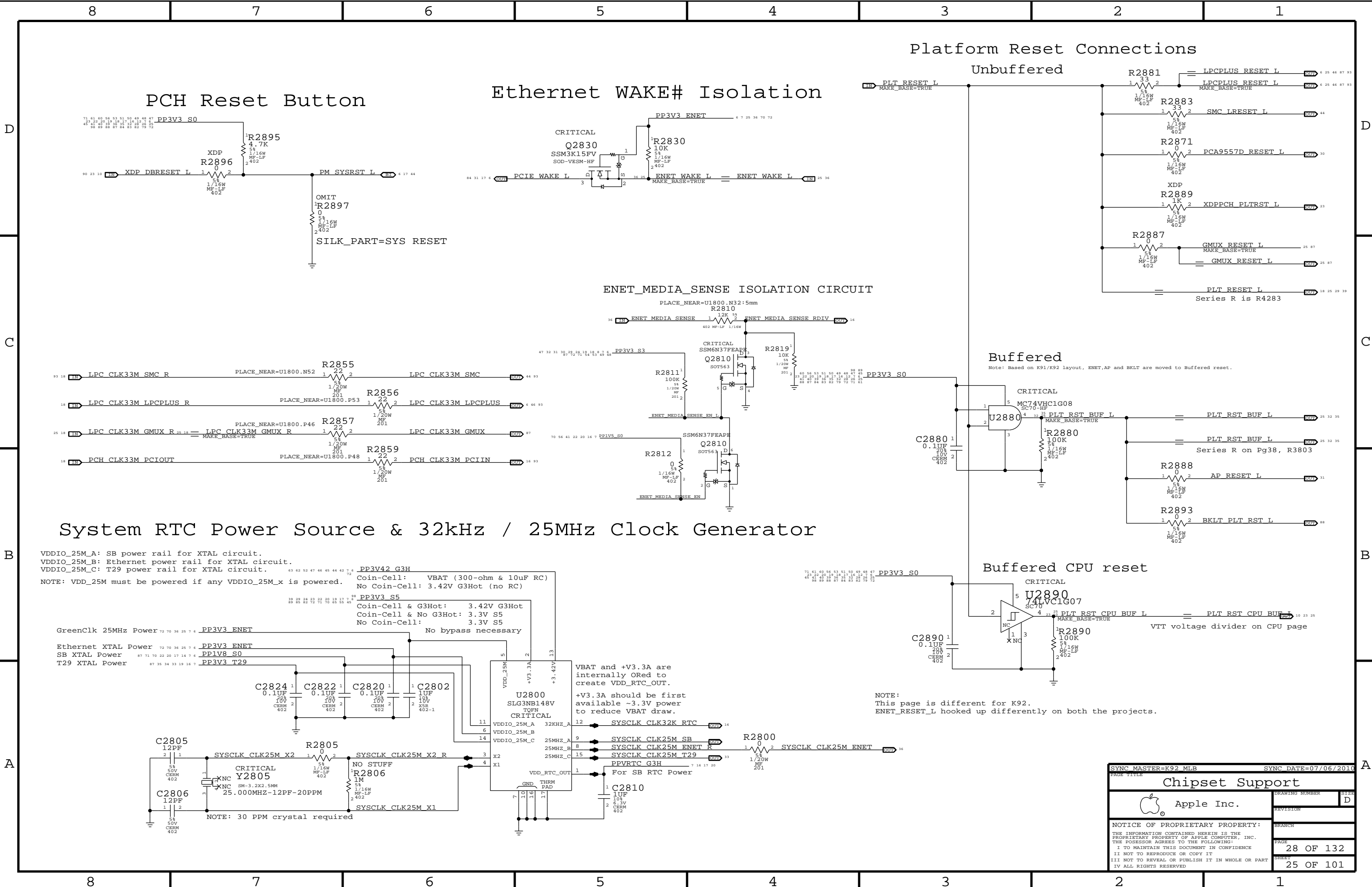
Trackpad/Keyboard

External A

SD Card/Express Card

SYNC MASTER=K91 ERICS SYNC DATE=10/08/2010

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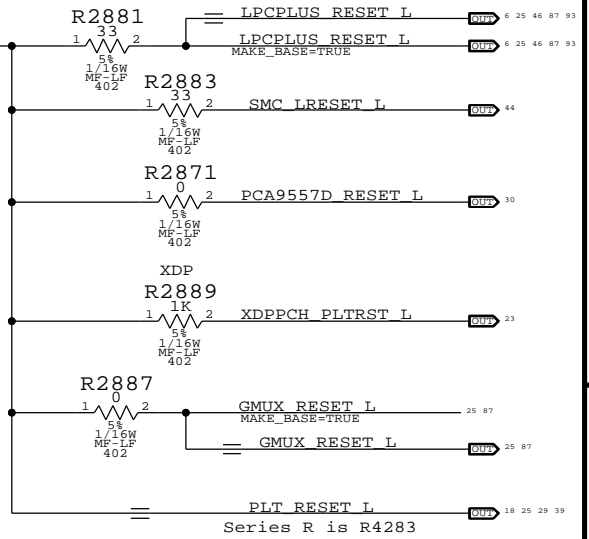


PCH Reset Button

Ethernet WAKE# Isolation

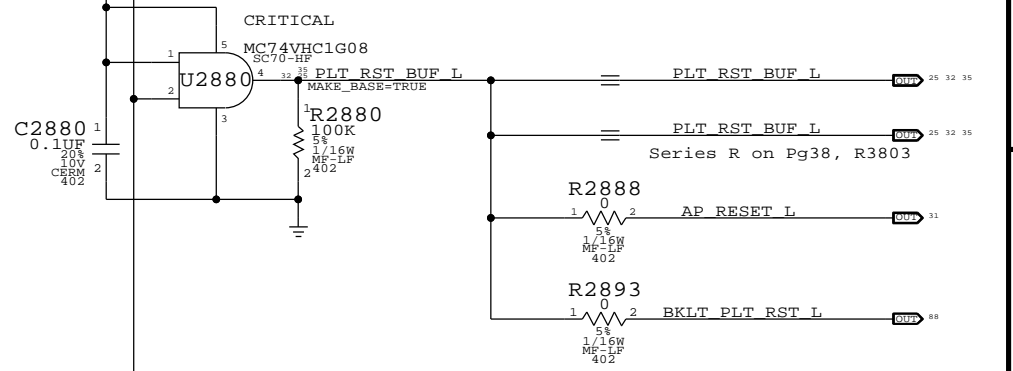
Platform Reset Connections

Unbuffered

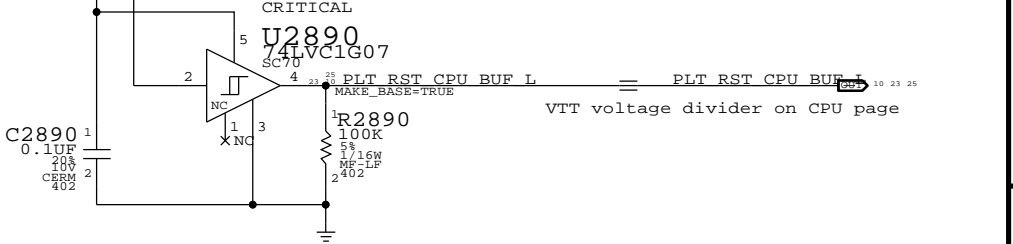


Buffered

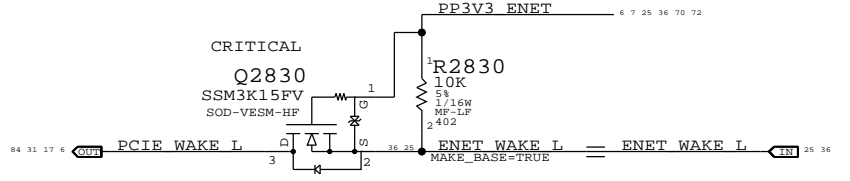
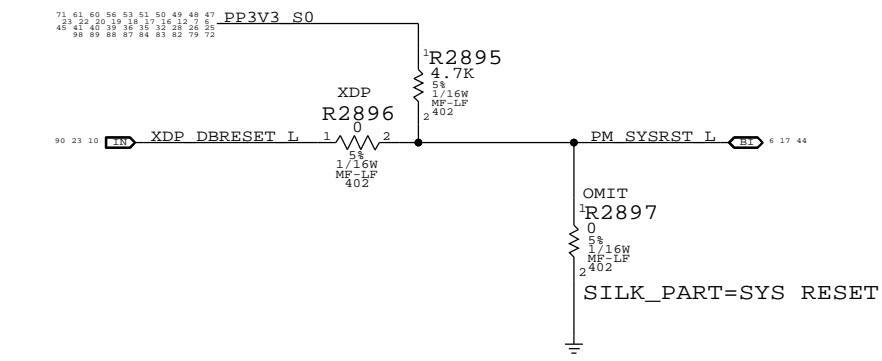
Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.



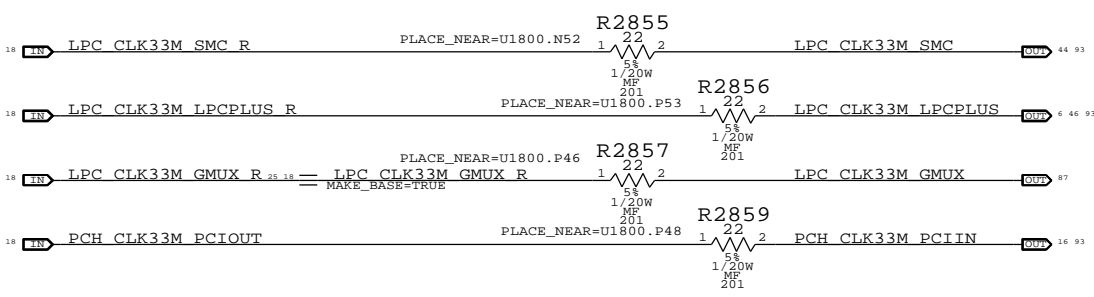
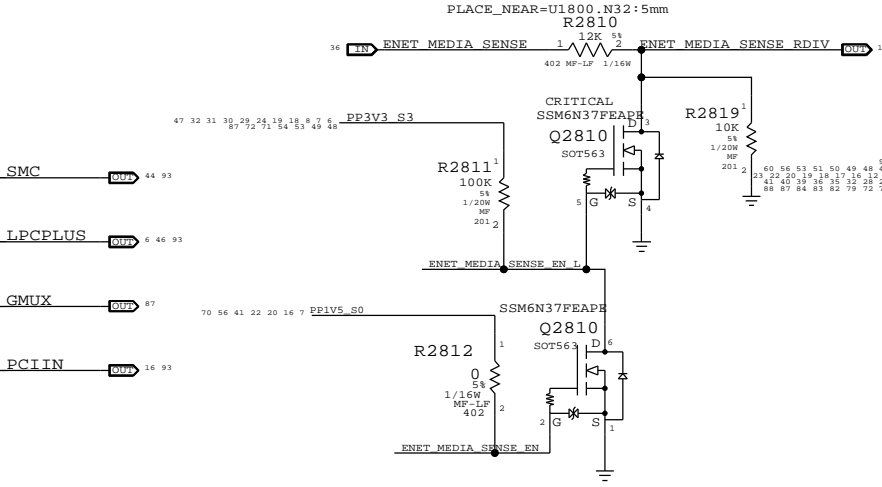
Buffered CPU reset



NOTE:
This page is different for K92.
ENET_RESET_L hooked up differently on both the projects.

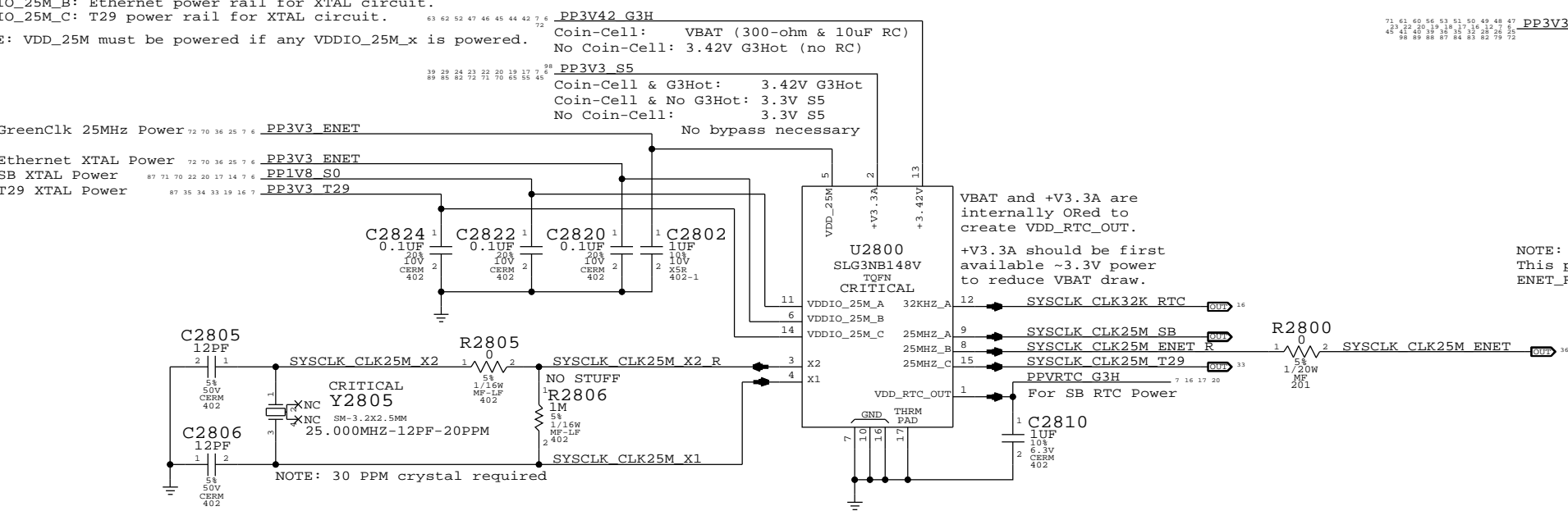



ENET_MEDIA_SENSE ISOLATION CIRCUIT



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



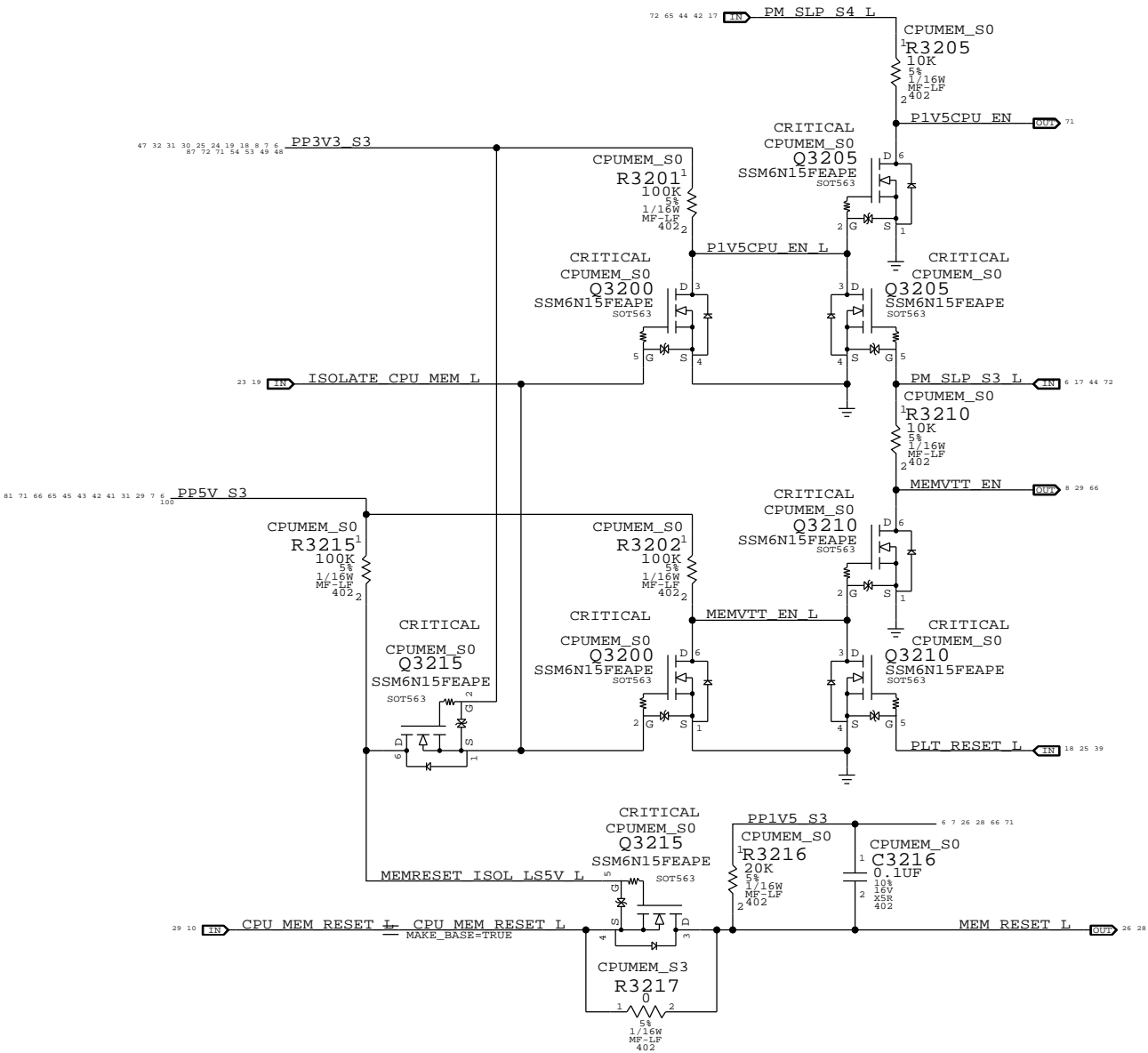
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Chipset Support			
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<table><tr><td colspan="8">CPU CHANNEL A DQS 0 -> DIMM A DQS 0</td><td colspan="8">CPU CHANNEL B DQS 0 -> DIMM B DQS 0</td></tr><tr><td colspan="8">MEM A DQS N<0> ==MEM A DQS N<0></td><td colspan="8">MEM B DQS N<0> ==MEM B DQS N<0></td></tr><tr><td colspan="8">MEM A DQS P<0> ==MEM A DQS P<0></td><td colspan="8">MEM B DQS P<0> ==MEM B DQS P<0></td></tr><tr><td colspan="8">MEM A DQ<7> ==MEM A DQ<3></td><td colspan="8">MEM B DQ<7> ==MEM B DQ<6></td></tr><tr><td colspan="8">MEM A DQ<6> ==MEM A DQ<6></td><td colspan="8">MEM B DQ<6> ==MEM B DQ<3></td></tr><tr><td colspan="8">MEM A DQ<5> ==MEM A DQ<5></td><td colspan="8">MEM B DQ<5> ==MEM B DQ<5></td></tr><tr><td colspan="8">MEM A DQ<4> ==MEM A DQ<4></td><td colspan="8">MEM B DQ<4> ==MEM B DQ<4></td></tr><tr><td colspan="8">MEM A DQ<3> ==MEM A DQ<7></td><td colspan="8">MEM B DQ<3> ==MEM B DQ<1></td></tr><tr><td colspan="8">MEM A DQ<2> ==MEM A DQ<0></td><td colspan="8">MEM B DQ<2> ==MEM B DQ<7></td></tr><tr><td colspan="8">MEM A DQ<1> ==MEM A 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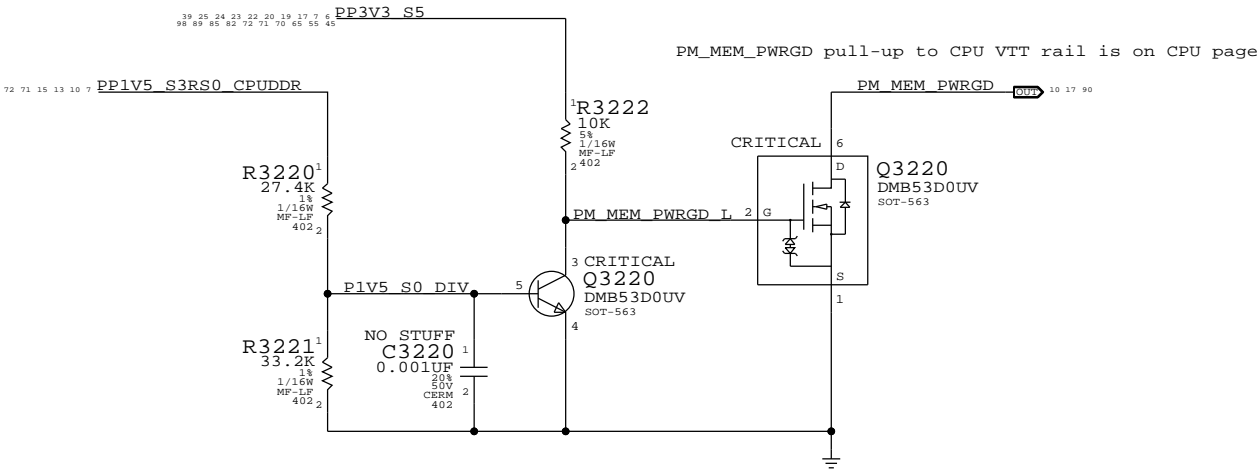
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

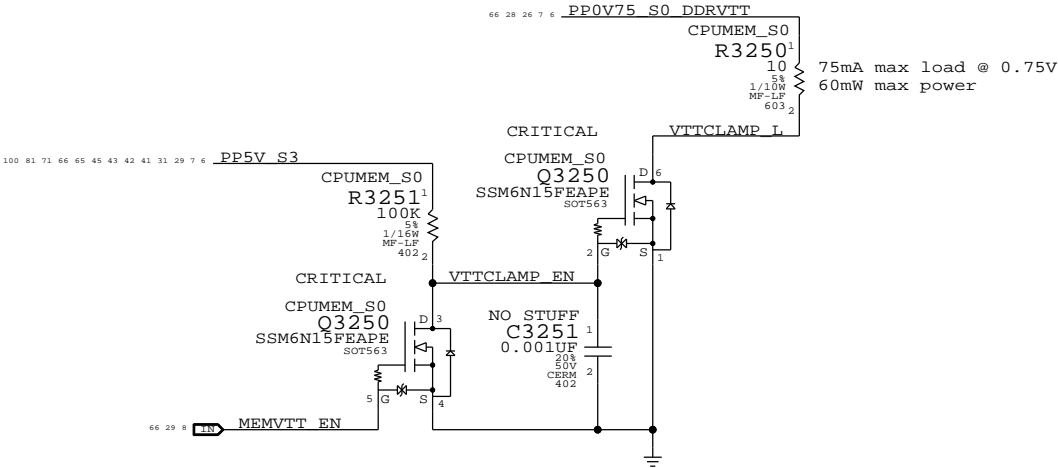


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp


Ensures CKE signals are held low in S3

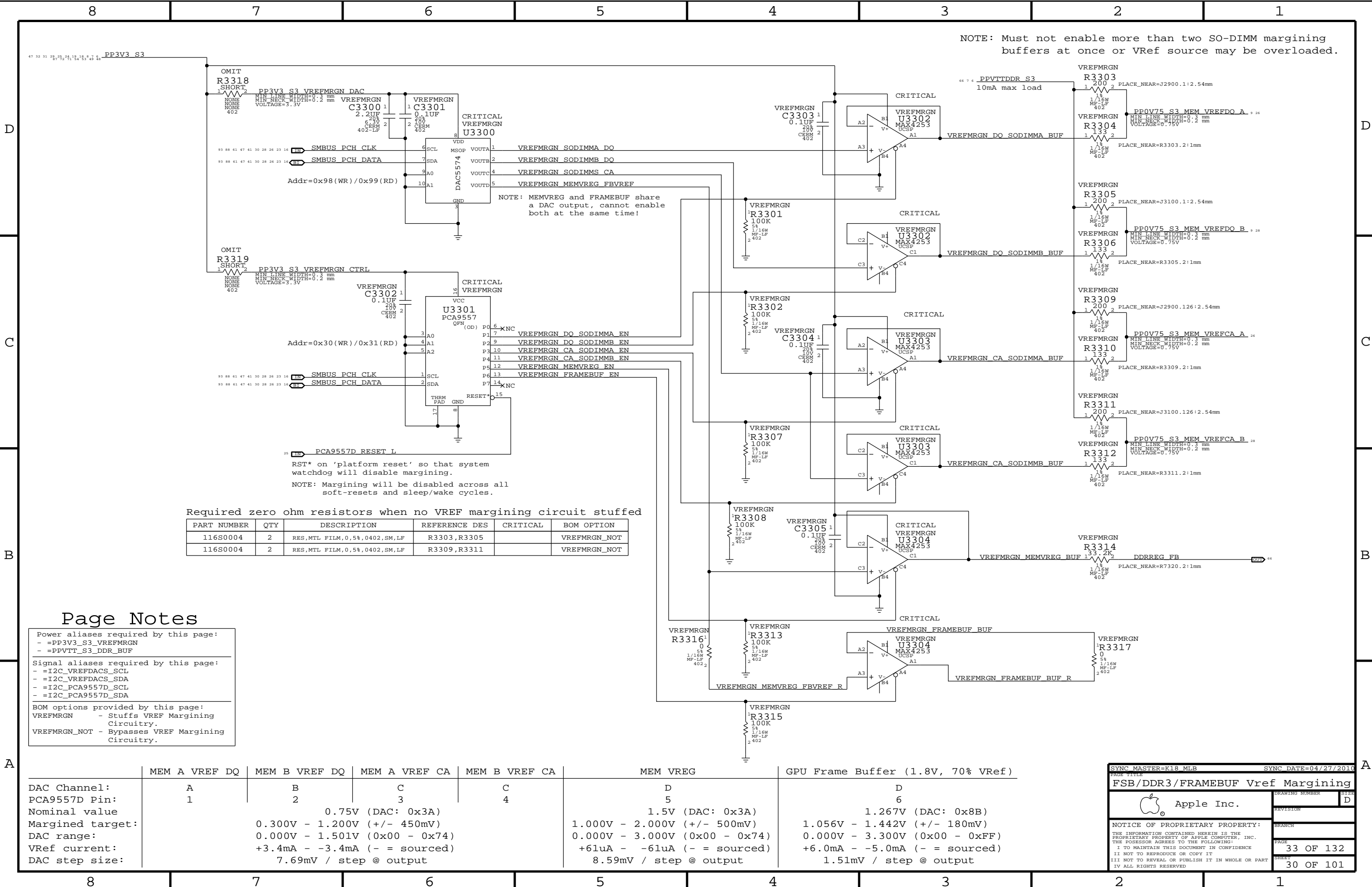


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K18 MLB		SYNC DATE=04/27/2010	
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CPU Memory S3 Support		DRAWING NUMBER	
 Apple Inc.		SIZE D	
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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value			0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:			0.300V - 1.200V (+/- 450mV)		1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:			0.000V - 1.501V (0x00 - 0x74)		0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:			+3.4mA - -3.4mA (- = sourced)		+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:			7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K18 MLB

SYNC DATE=04/27/2010

FSB/DDR3/FRAMEBUF Vref Margining

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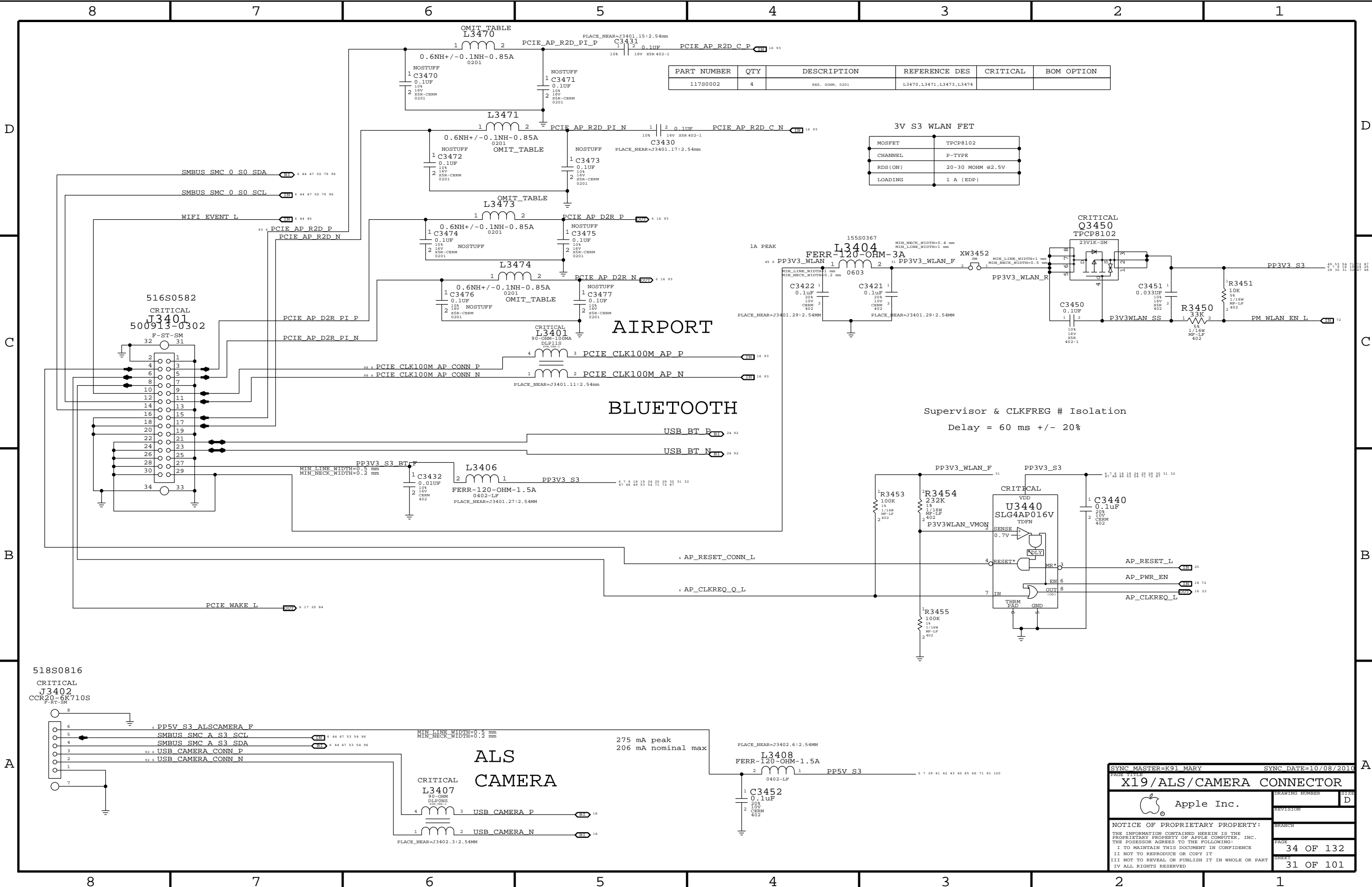
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PAGE

SHEET

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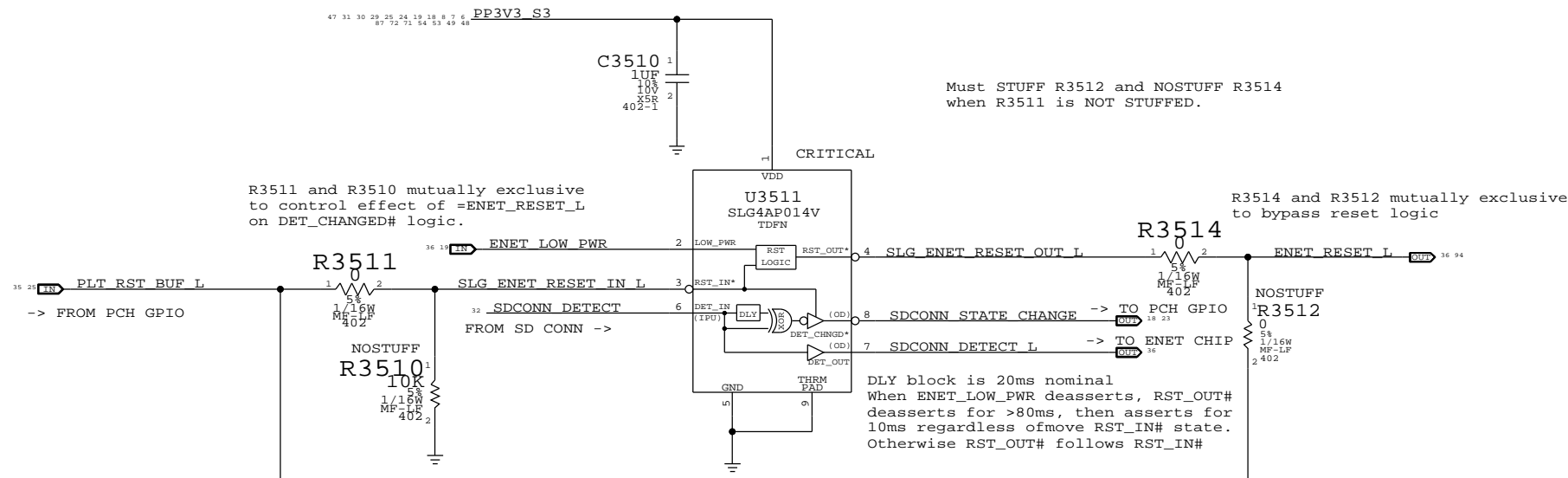
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 008M, 0201	L3470,L3471,L3473,L3474		


3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

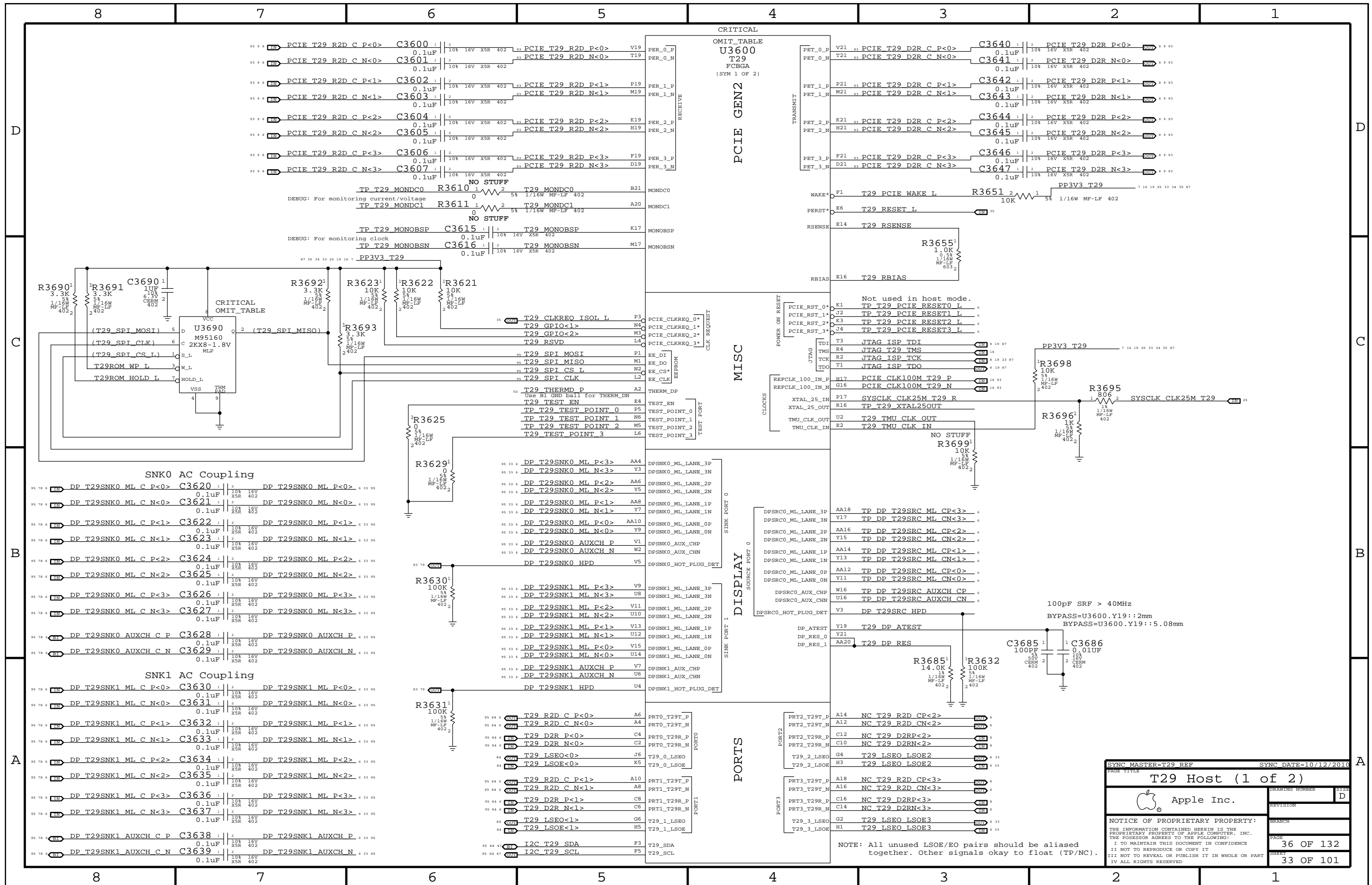
Supervisor & CLKFREG # Isolation
Delay = 60 ms +/- 20%

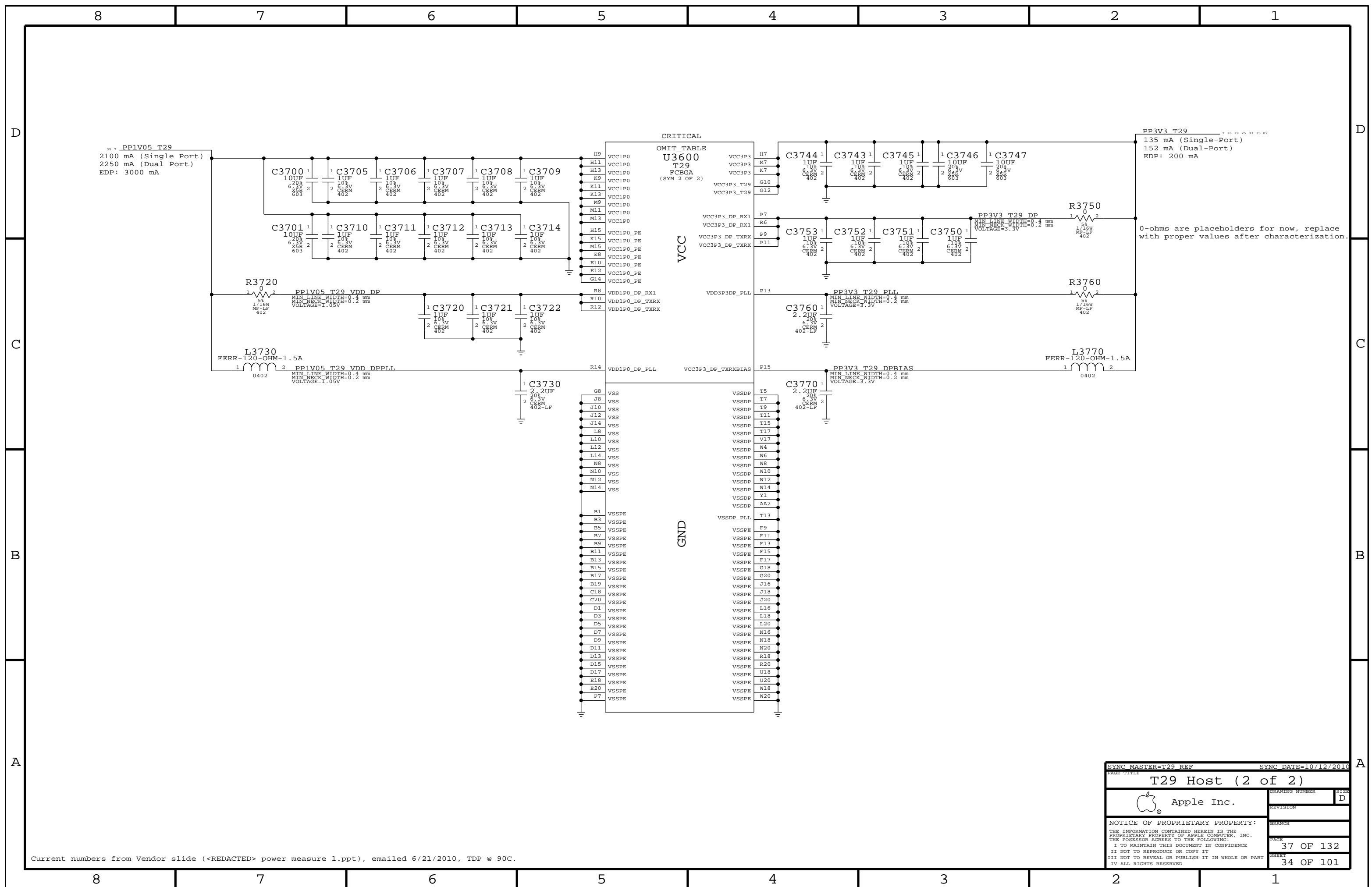
SYNC MASTER=K91 MARY		SYNC DATE=10/08/2010	
PAGE TITLE		X19/ALS/CAMERA CONNECTOR	
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		PAGE	34 OF 132
		SHEET	31 OF 101

TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.

[illegible]

SYNCH MASTER=K91 ERICSYNCH DATE=10/08/2010		A	
SD READER CONNECTOR			
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		SHEET 32 OF 101	





8	7	6	5	4	3	2	1
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8	7	6	5	4	3	2	1
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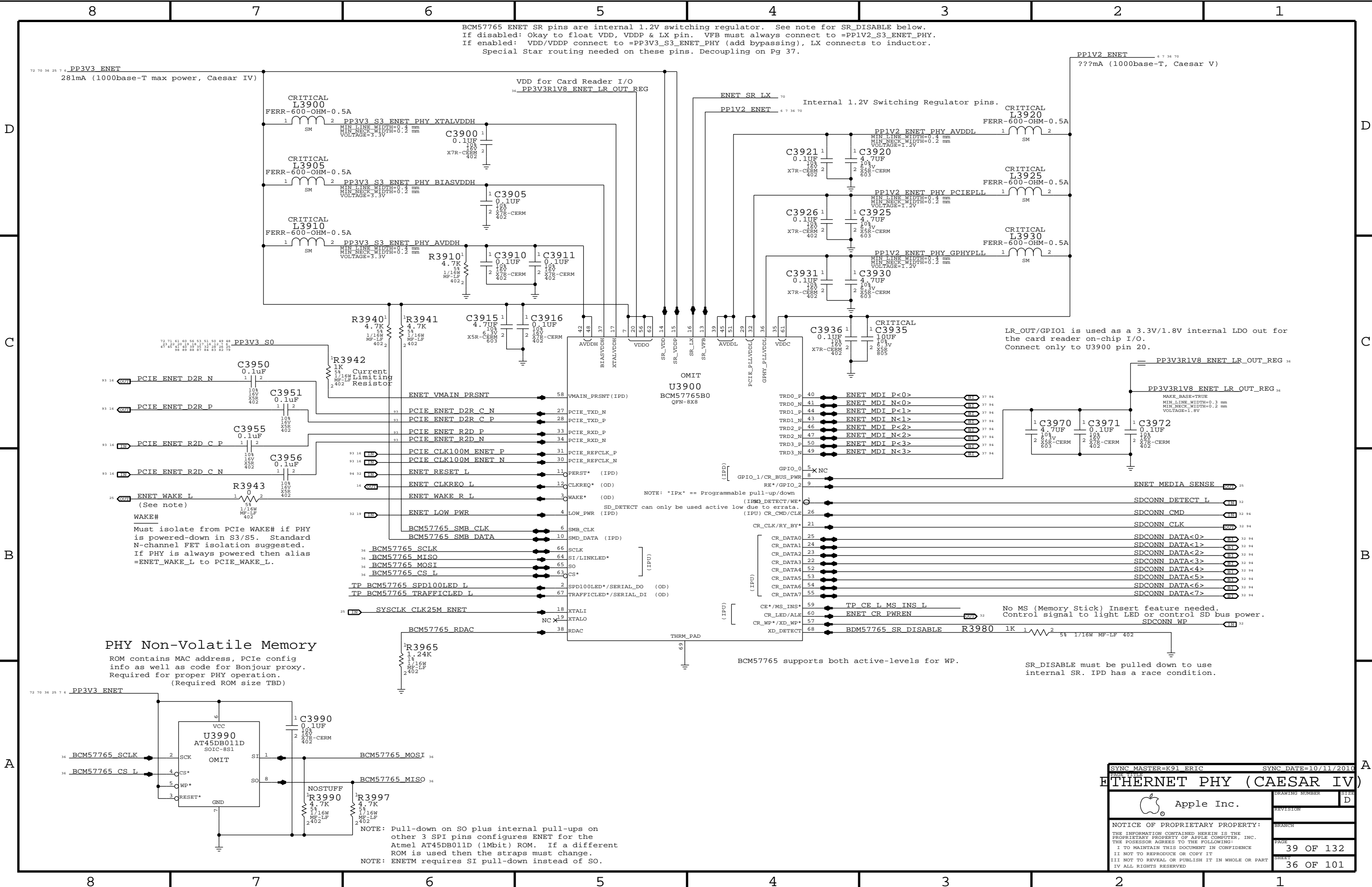
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8	7	6	5	4	3	2	1
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A



BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP1V2 ENET
???mA (1000base-T, Caesar V)

PP3V3 ENET
281mA (1000base-T max power, Caesar IV)

Internal 1.2V Switching Regulator pins.

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O. Connect only to U3900 pin 20.

PHY Non-Volatile Memory
ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)

BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

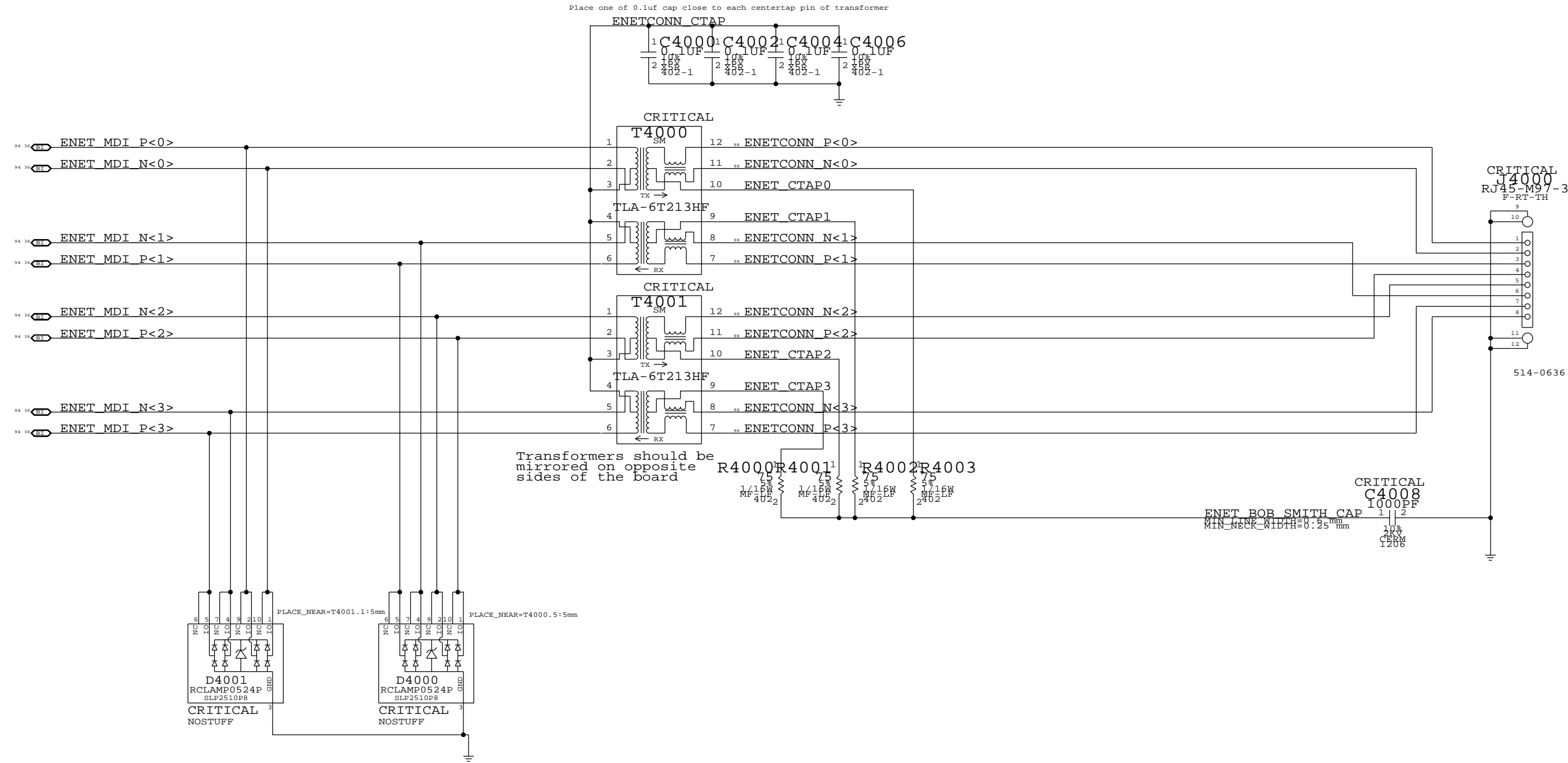
SYNC MASTER=K91.ERIC		SYNC DATE=10/11/2010	
PAGE TITLE		ETHERNET PHY (CAESAR IV)	
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
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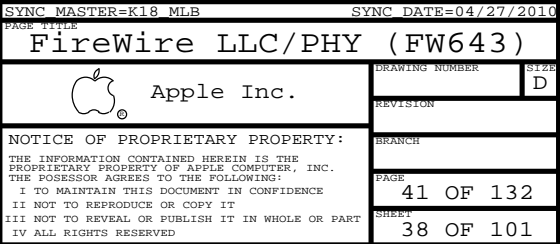
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K91 TRINHNT		SYNC DATE=05/26/2010	
PAGE TITLE			
Ethernet Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
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Page Notes

Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

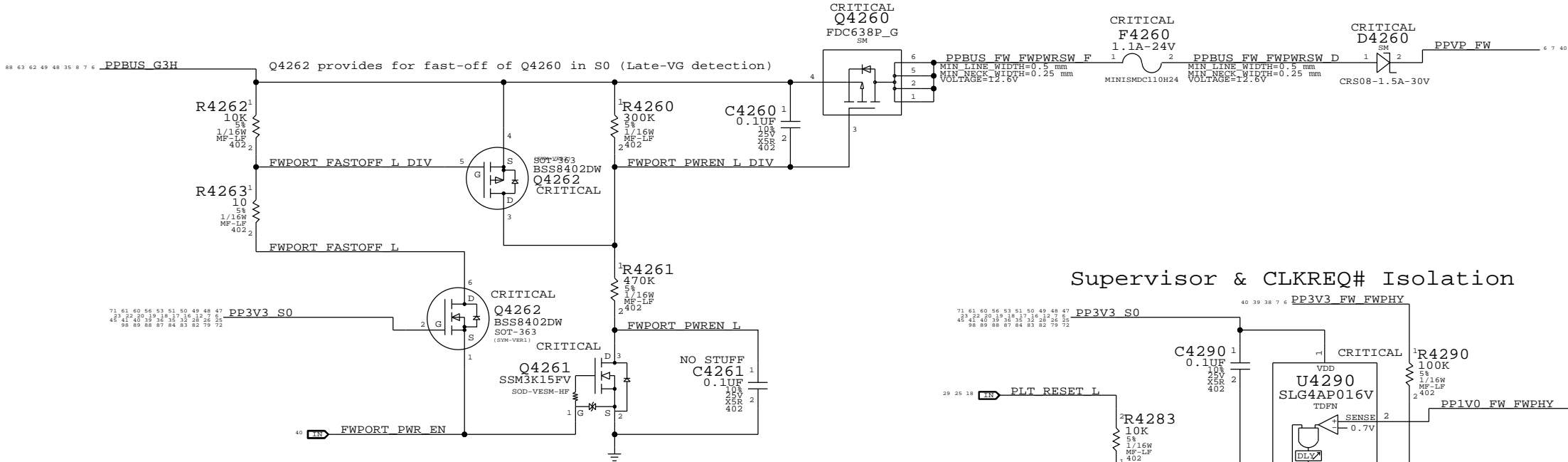
Signal aliases required by this page:

- =FW_CLKREQ_L
- =FW_PME_L

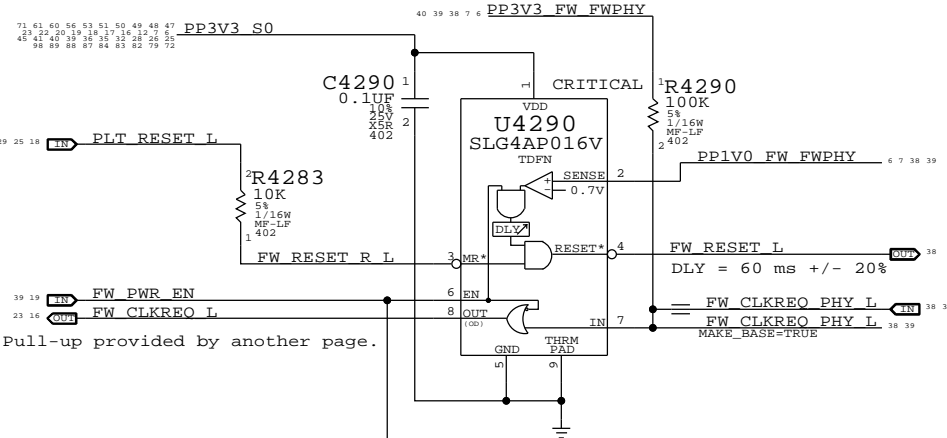
BOM options provided by this page:

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FireWire Port Power Switch

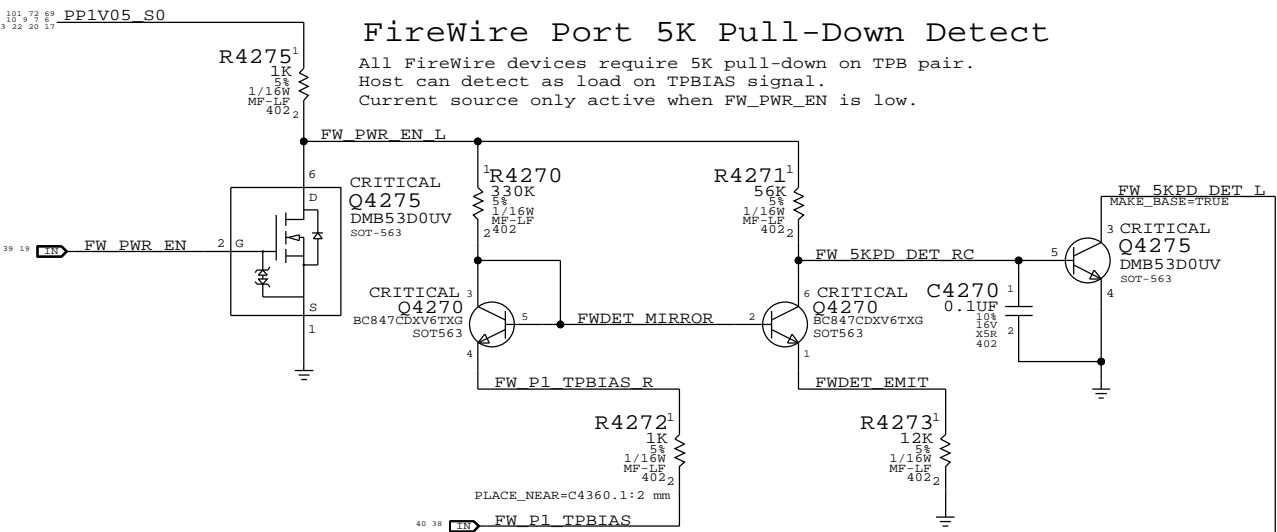


Supervisor & CLKREQ# Isolation



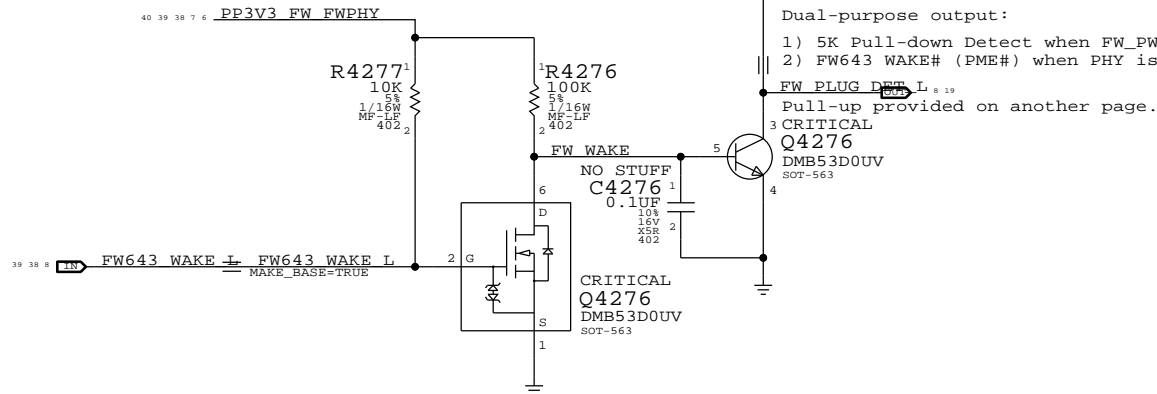
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

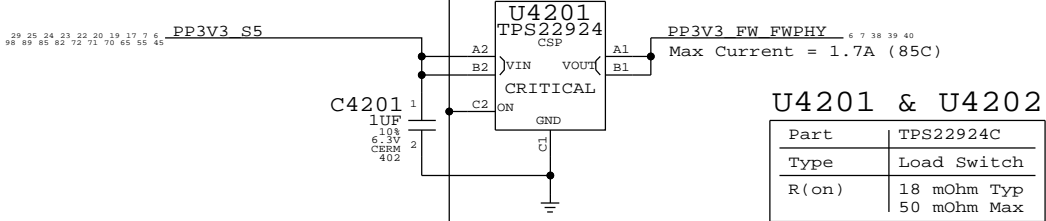
When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.



- Dual-purpose output:
- 1) 5K Pull-down Detect when FW_PWR_EN is low.
 - 2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

3.3V FW Switch

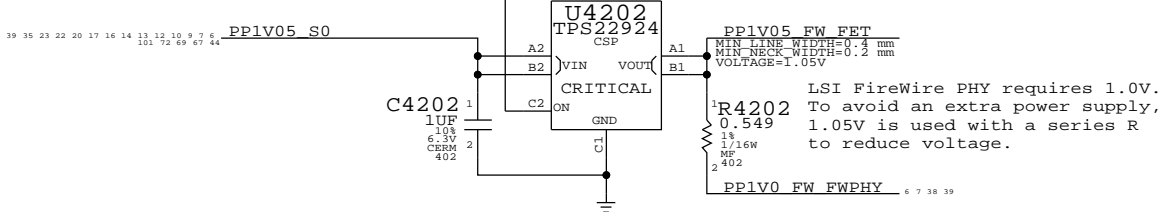



U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



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PAGE TITLE		FireWire Port & PHY Power	
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		PAGE	42 OF 132
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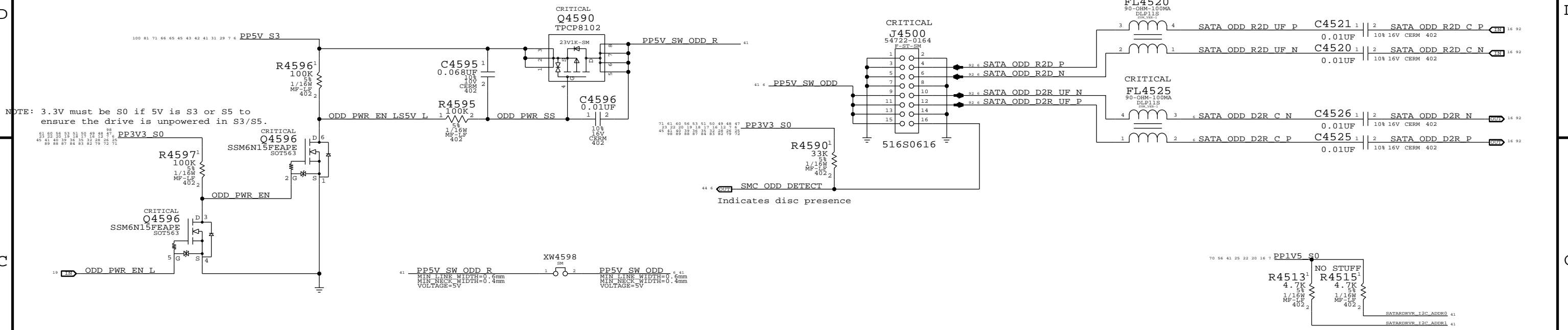
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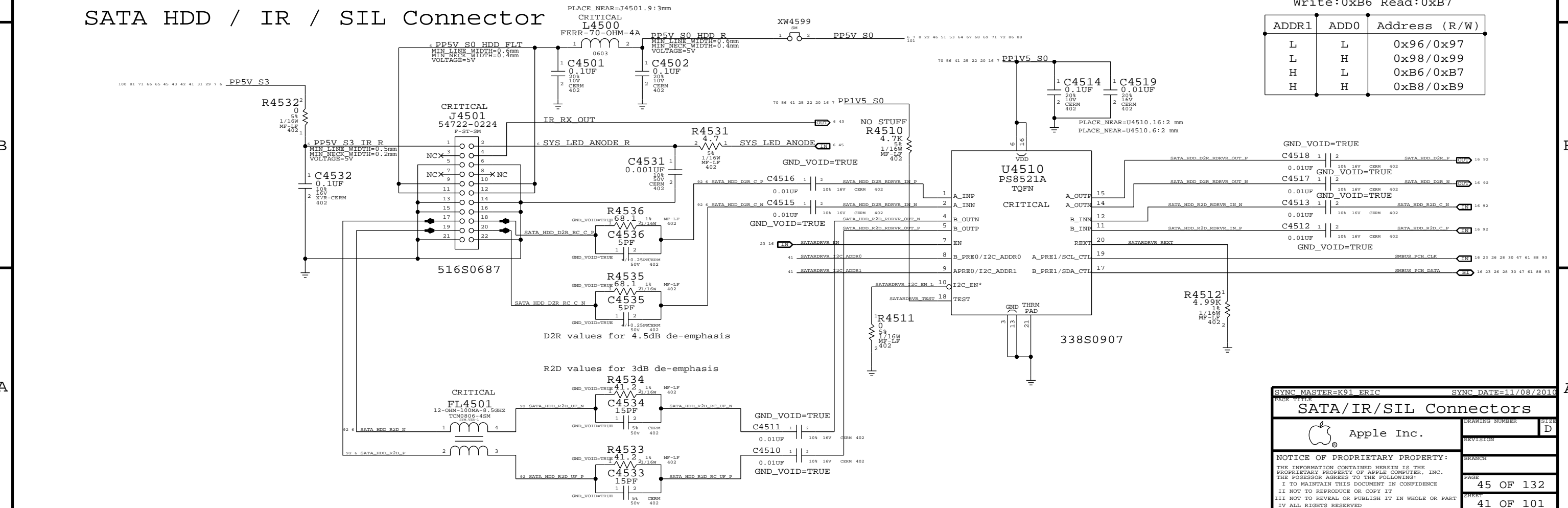
A

SATA ODD Connector

ODD Power Control



SATA HDD / IR / SIL Connector



SYNC MASTER=K91.ERIC

SYNC DATE=11/08/2010

SATA/IR/SIL Connectors

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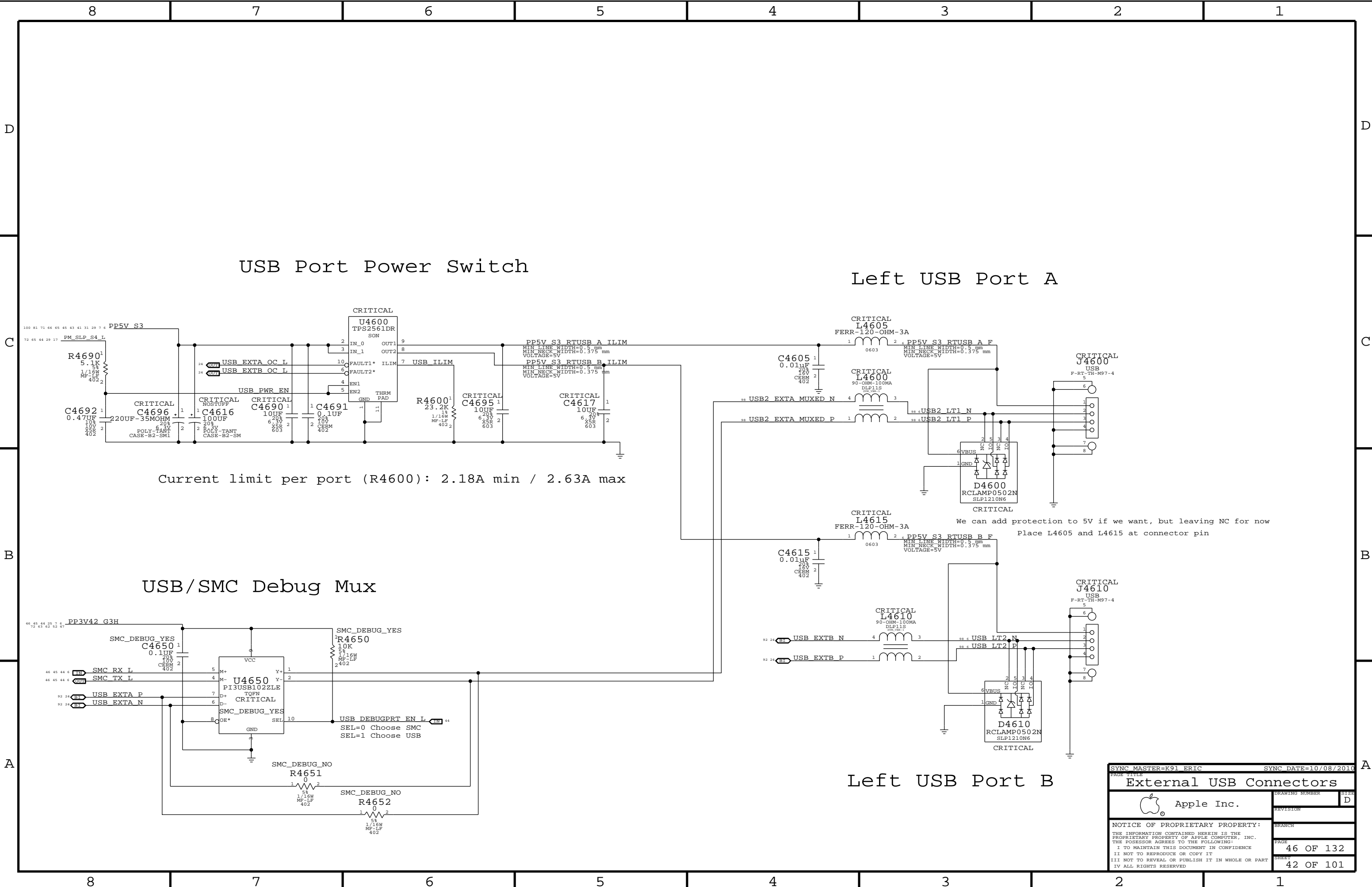
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USB Port Power Switch


Left USB Port A

USB/SMC Debug Mux

Left USB Port B

Current limit per port (R4600): 2.18A min / 2.63A max

We can add protection to 5V if we want, but leaving NC for now
Place L4605 and L4615 at connector pin

SYNC MASTER=K91.ERIC		SYNC DATE=10/08/2010	
PAGE TITLE			
External USB Connectors			
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8 7 6 5 4 3 2 1

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8 7 6 5 4 3 2 1

IR SUPPORT

PP5V_S3

C4801
0.1UF
105
50V
X7R-CERM
402

U4800
CY7C63803-LQXC
QFN

USB_IR_P
DIFFERENTIAL_PAIR=USB2_IR_P
USB_IR_N
DIFFERENTIAL_PAIR=USB2_IR_N
IR_VREF_FILTER

C4803
1UF
105
50V
X5C-1

CRITICAL
OMIT

P/N 338S0633

THRML
PAD

VSS

IR_RX_OUT_RC

R4800
100
5%
1/16W
MF-F
402

C4804
0.001UF
105
50V
CERM
402

IR_RX_OUT

41

SYNC MASTER=K18_MLB SYNC DATE=04/27/2010

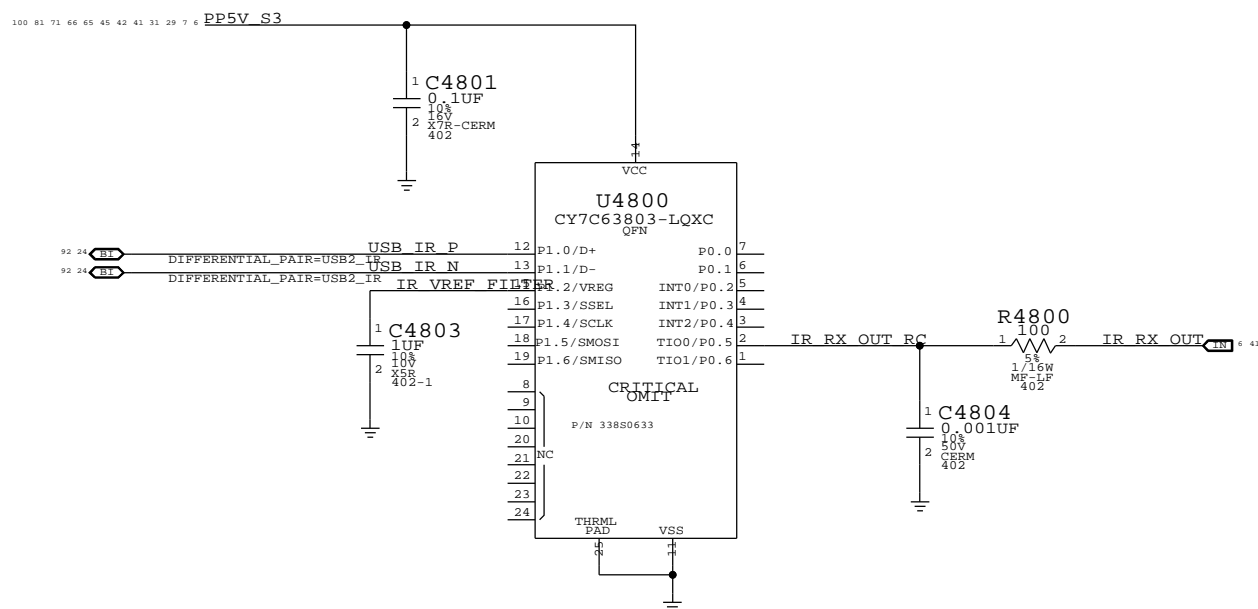
Front Flex Support

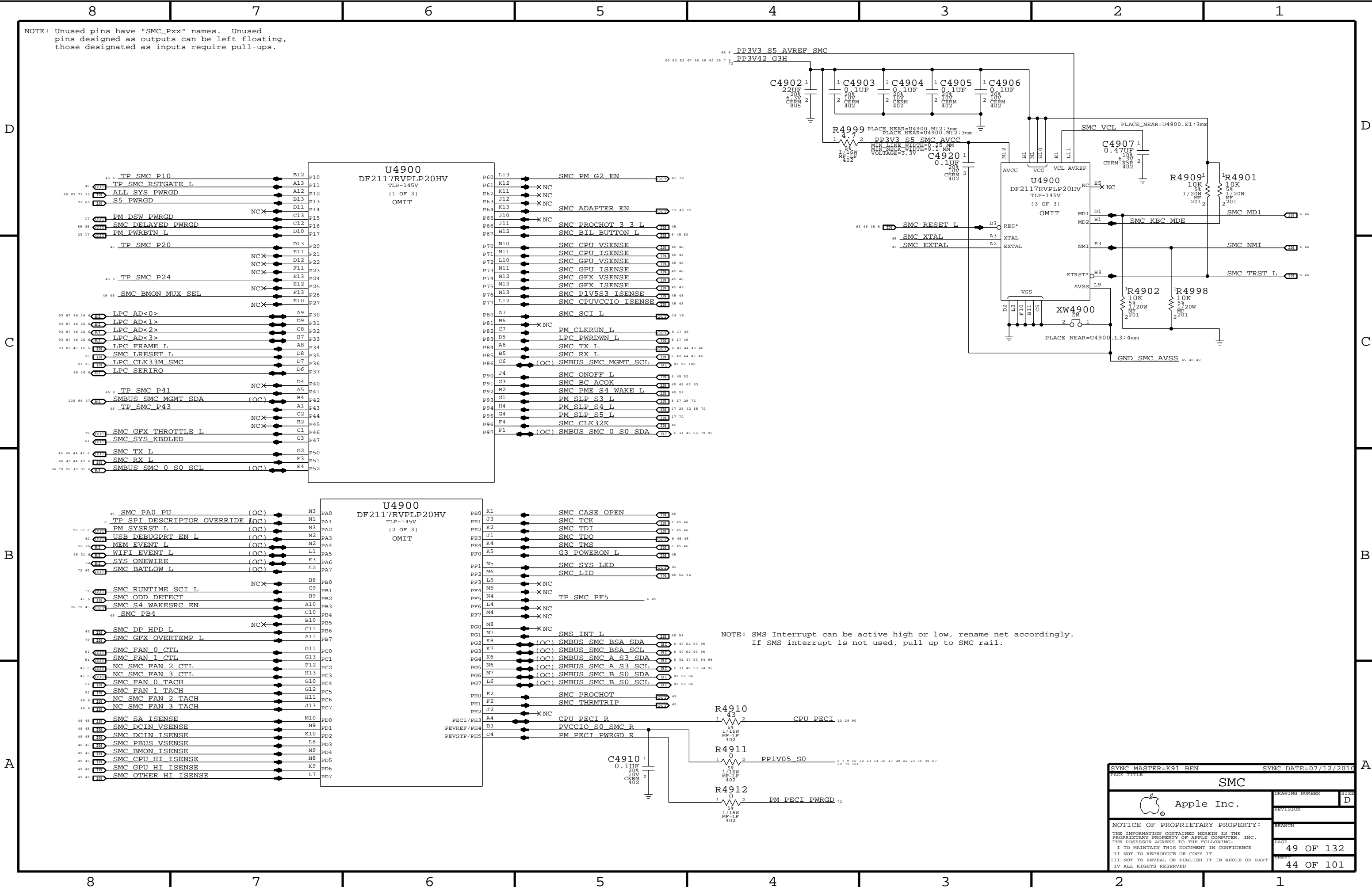
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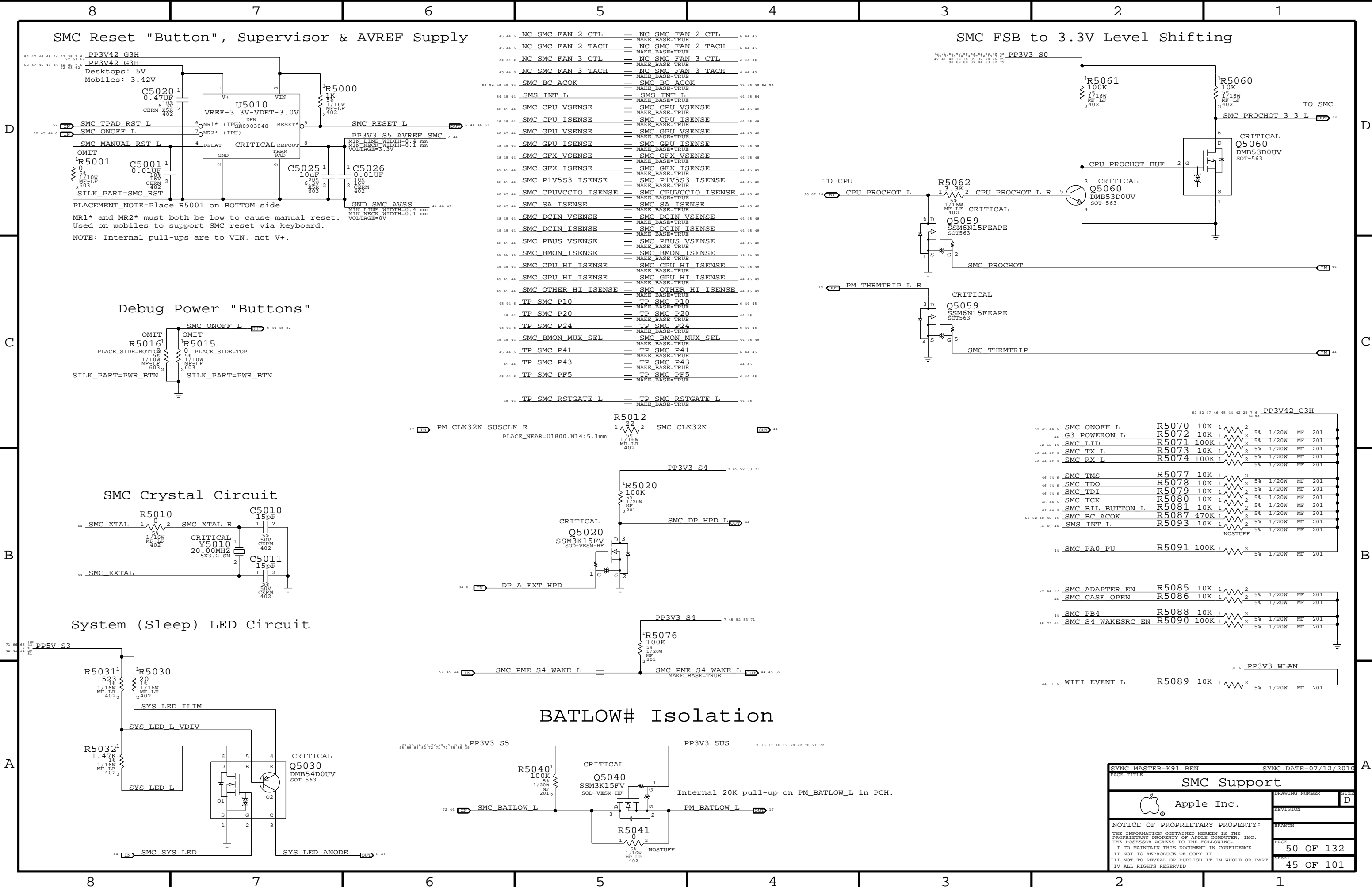
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SMC Support

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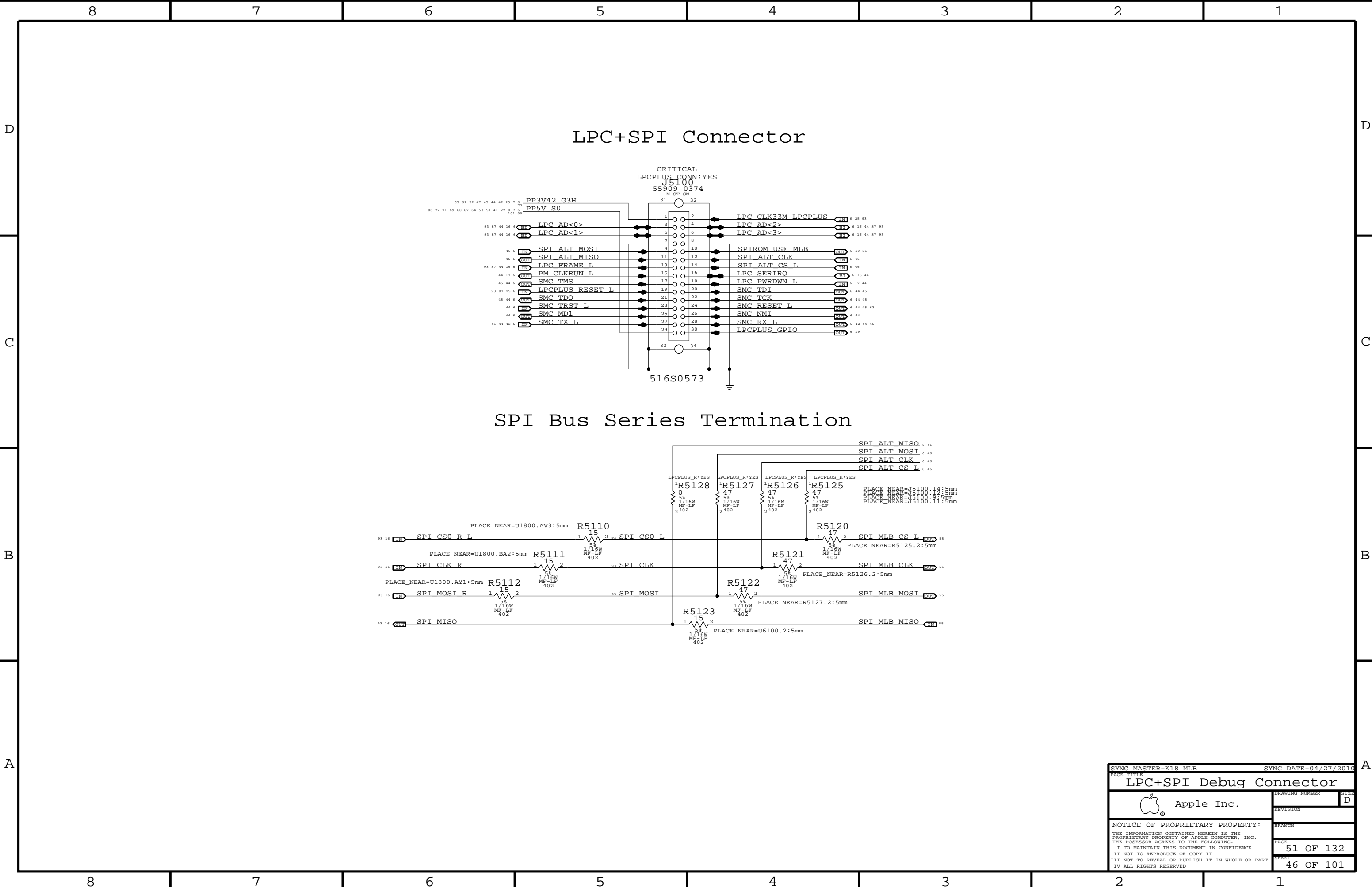
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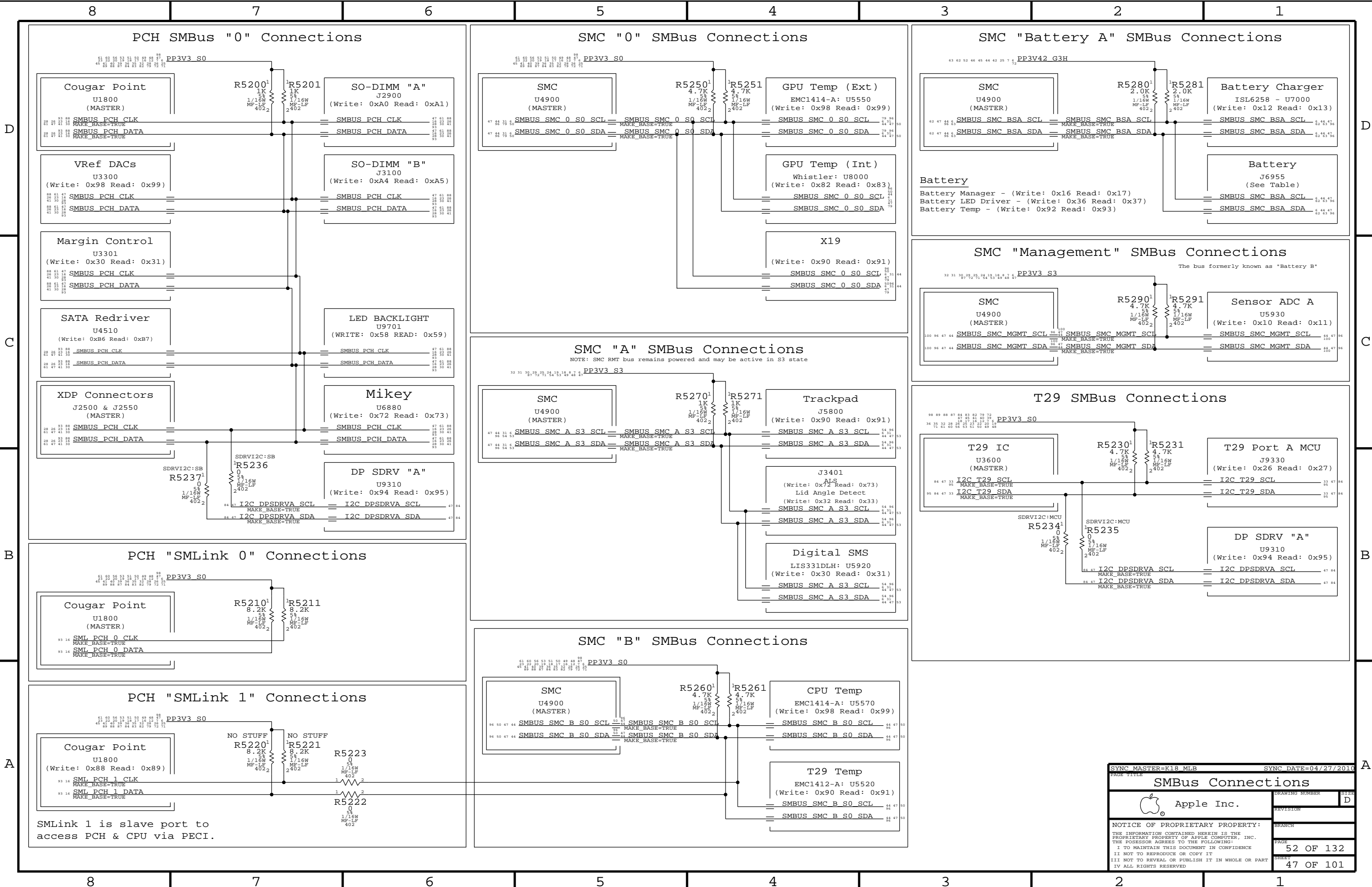
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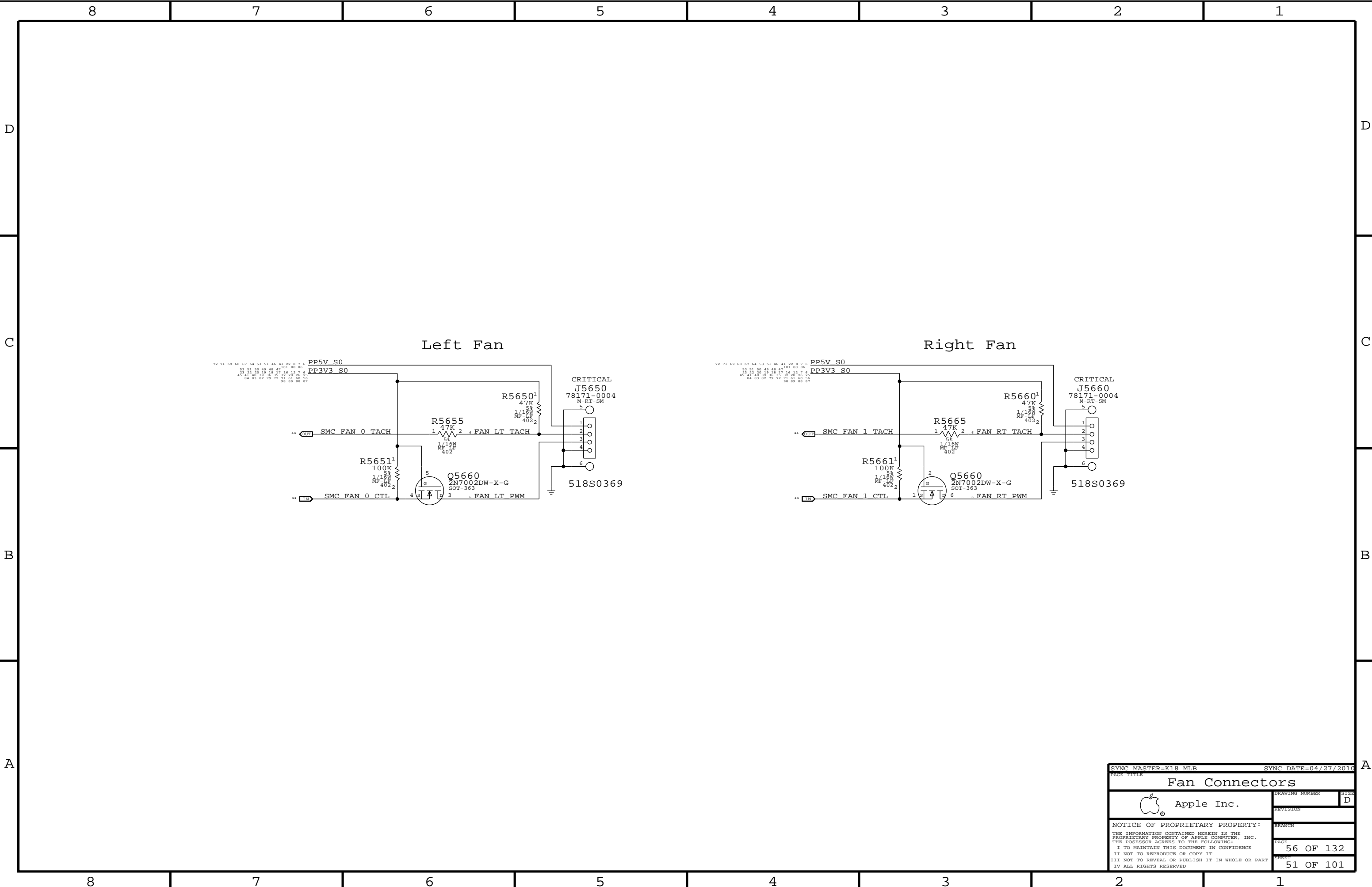


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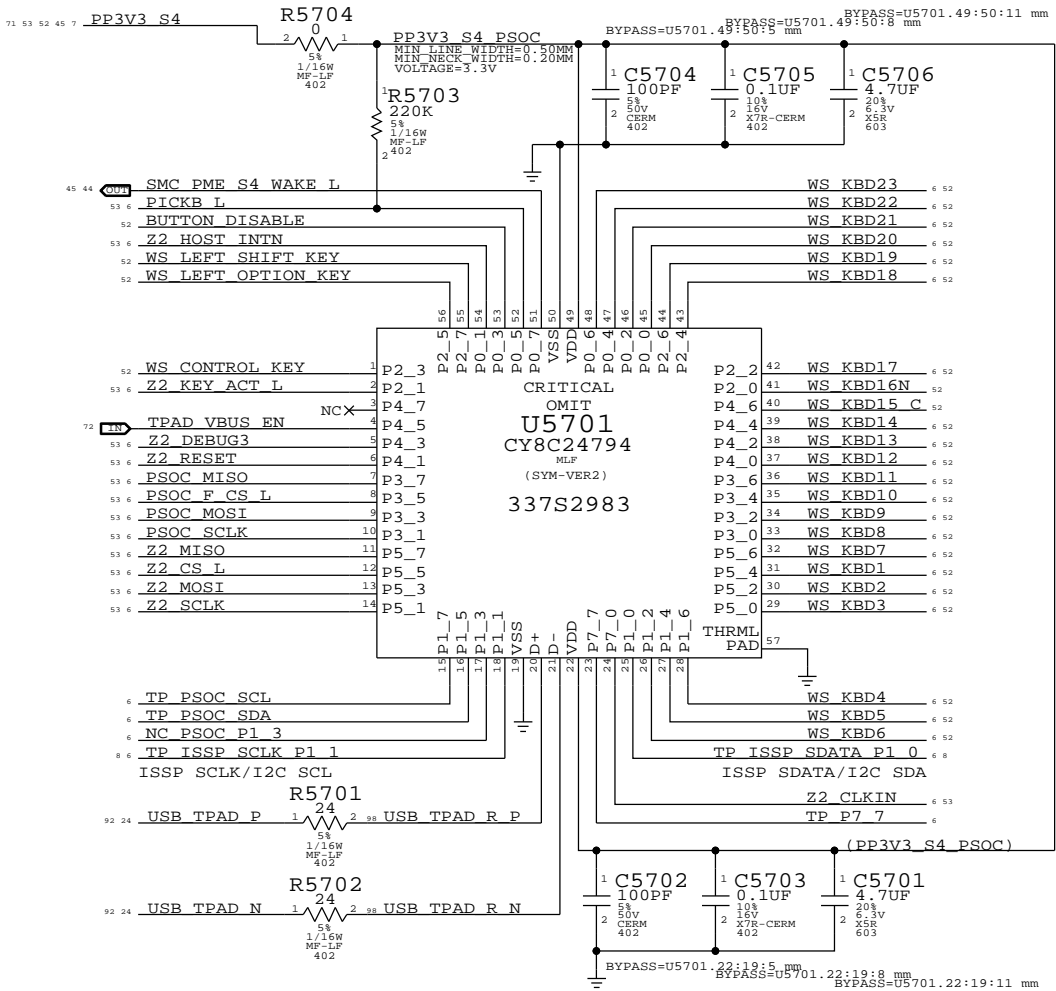
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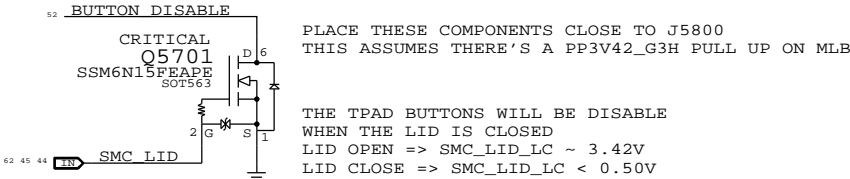


PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

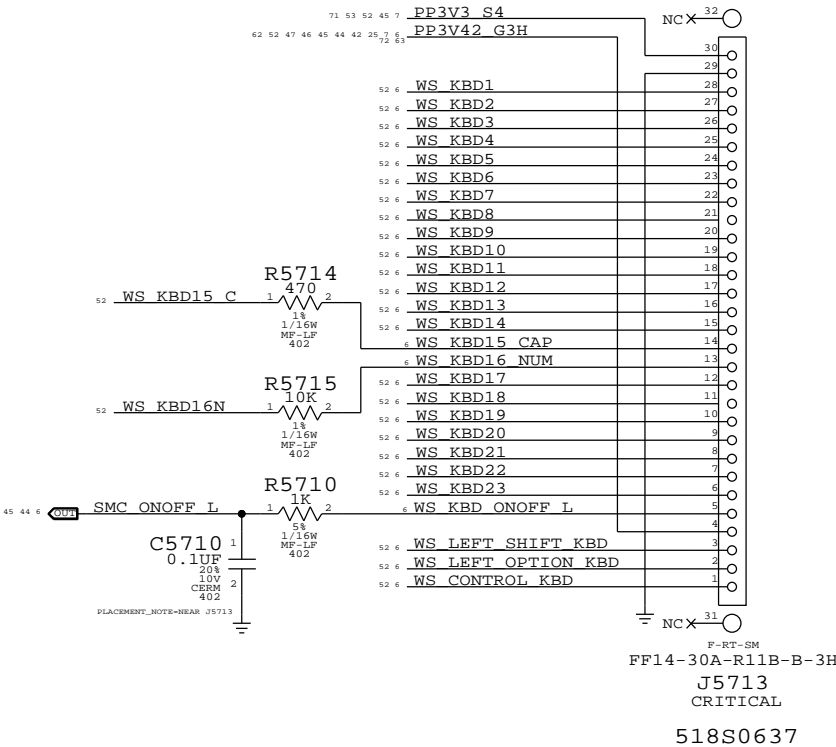


TPAD Buttons Disable



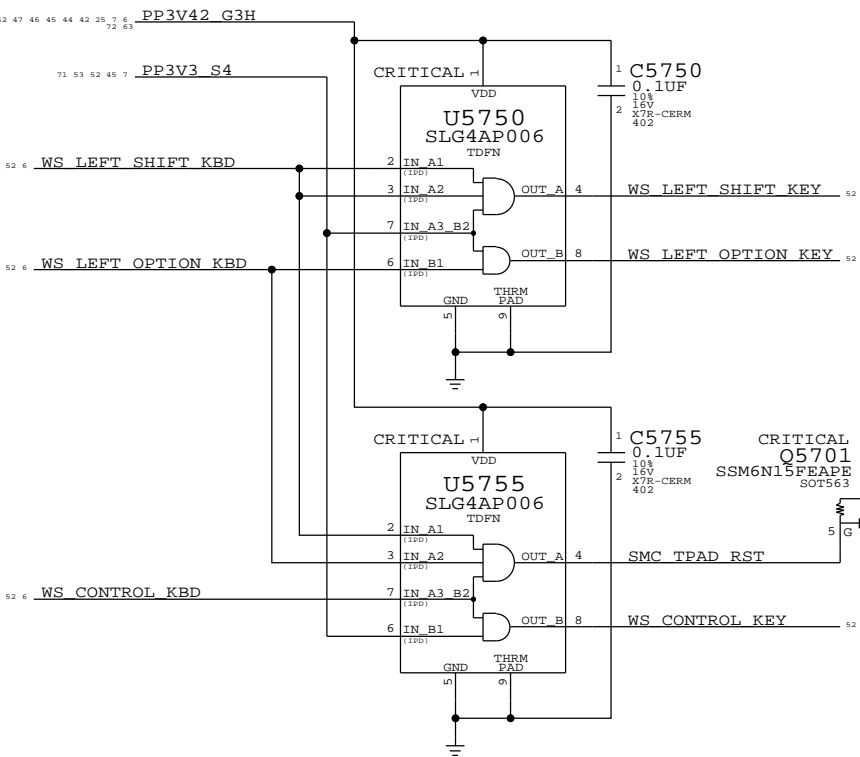
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
	VOUT	80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	VOUT	14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector



SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDed with PSOC power to isolate when PSOC is not powered.

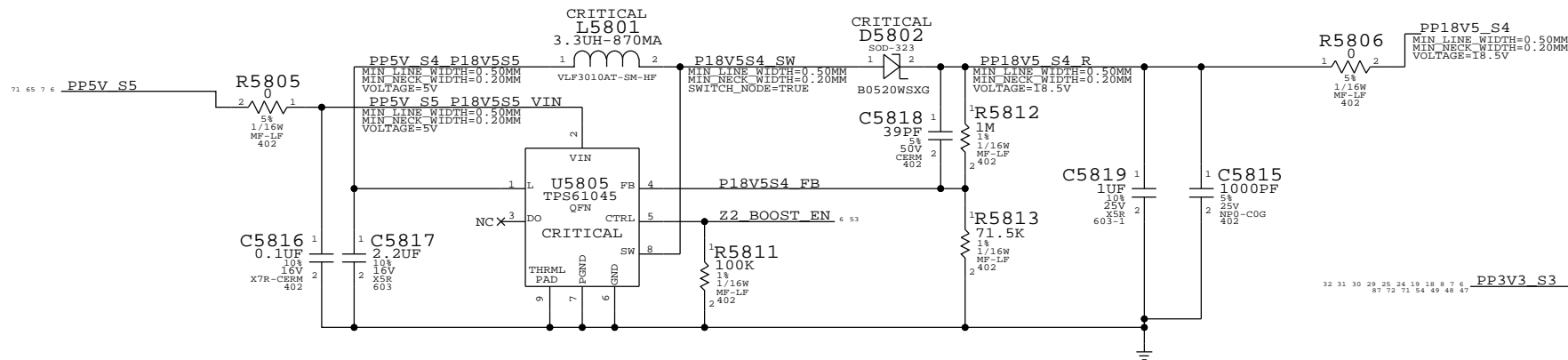


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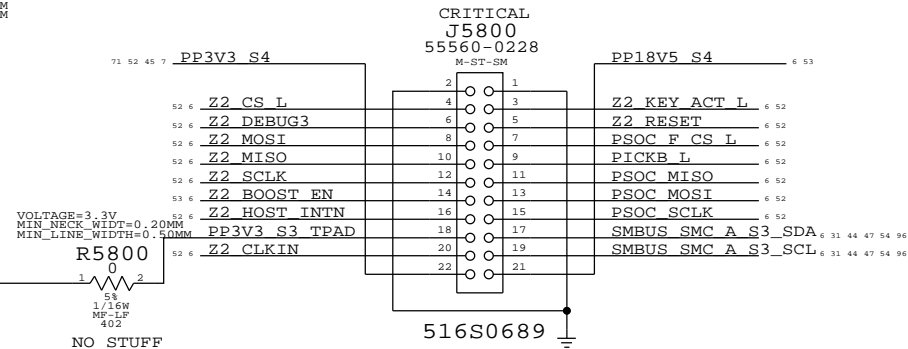
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:

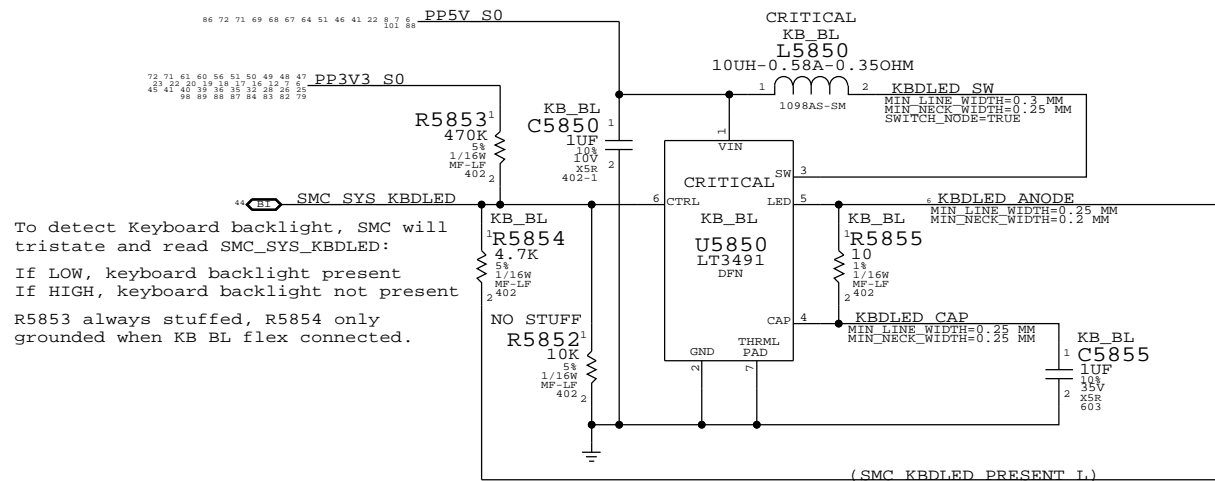
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector

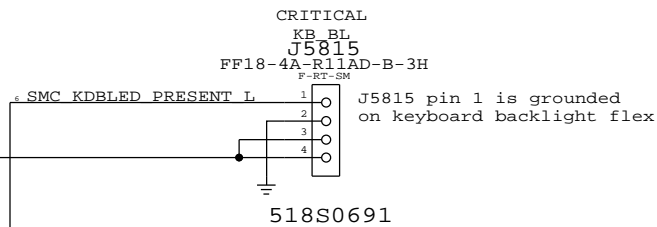


Keyboard Backlight Driver & Detection

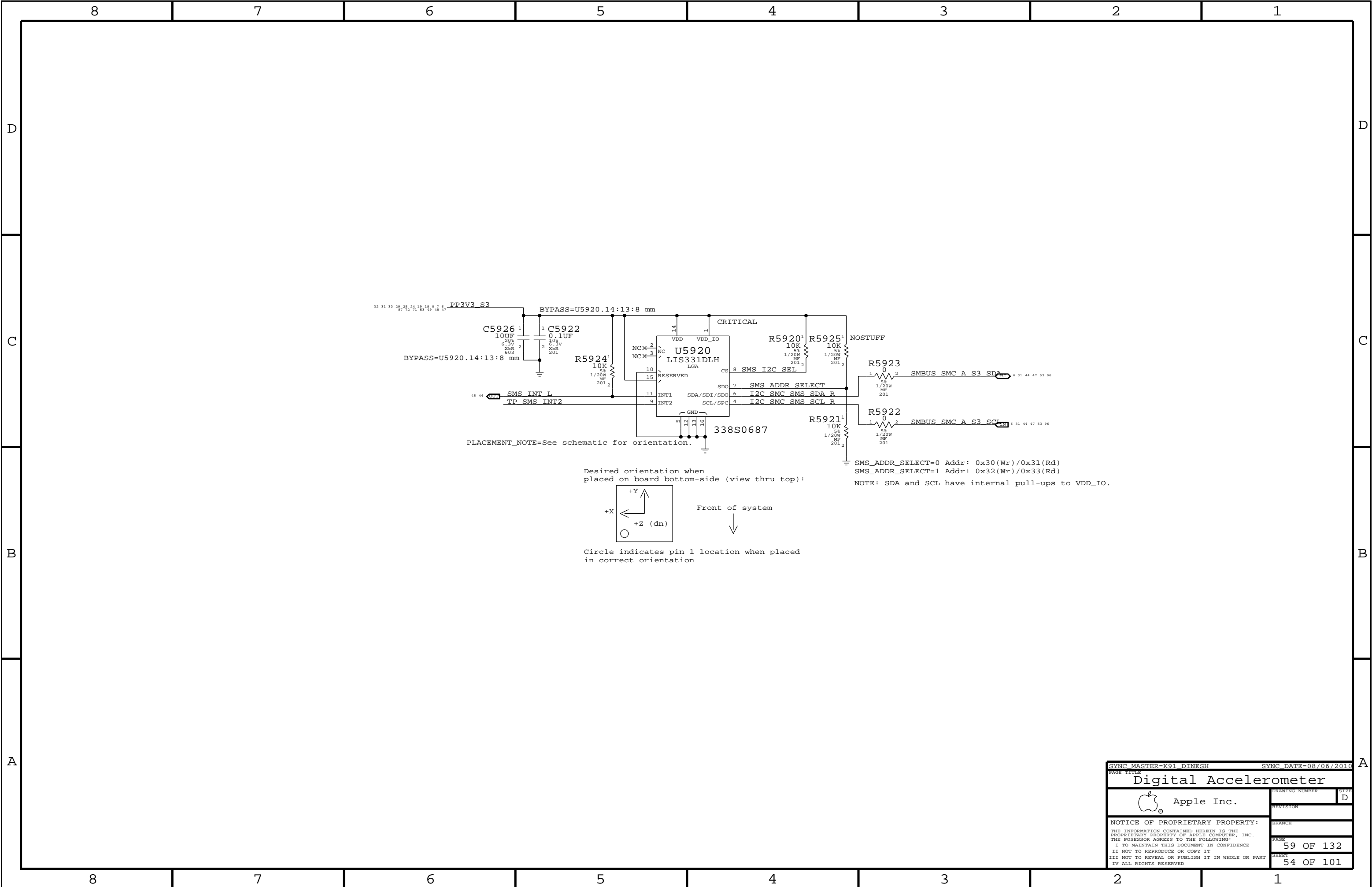


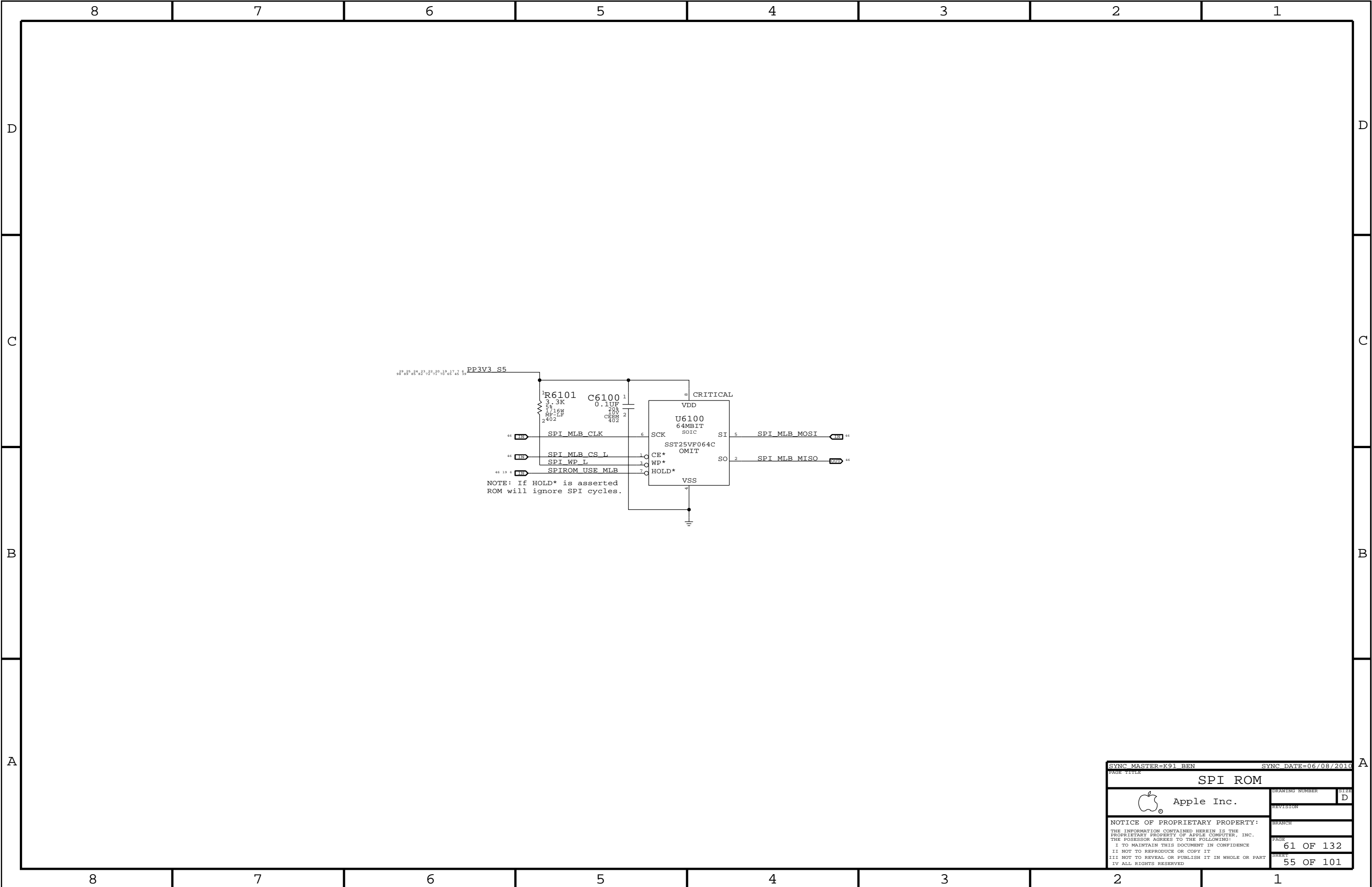
To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

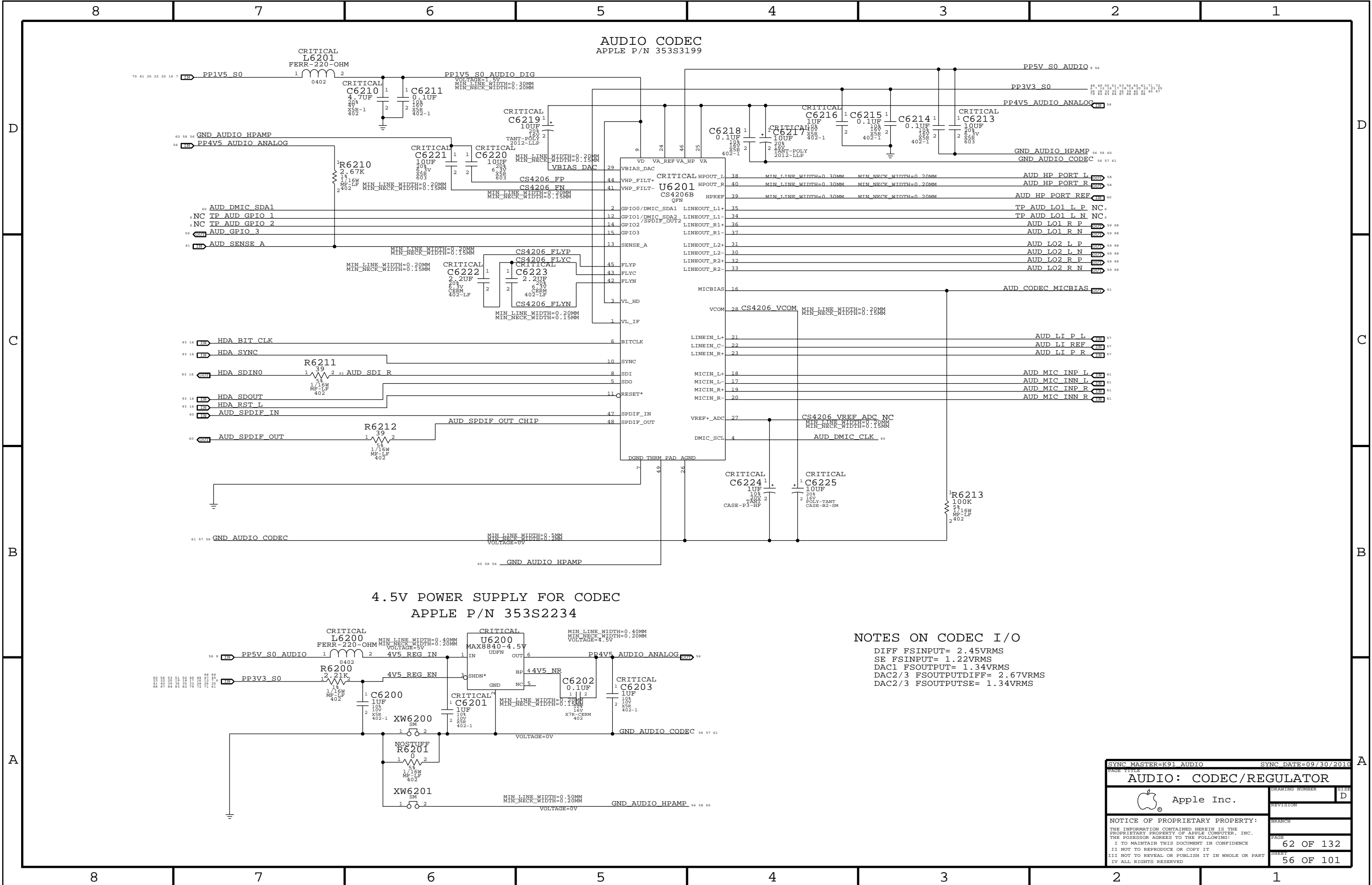
Keyboard Backlight Connector



SYNC MASTER=K91.ERIC		SYNC DATE=07/14/2010	
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


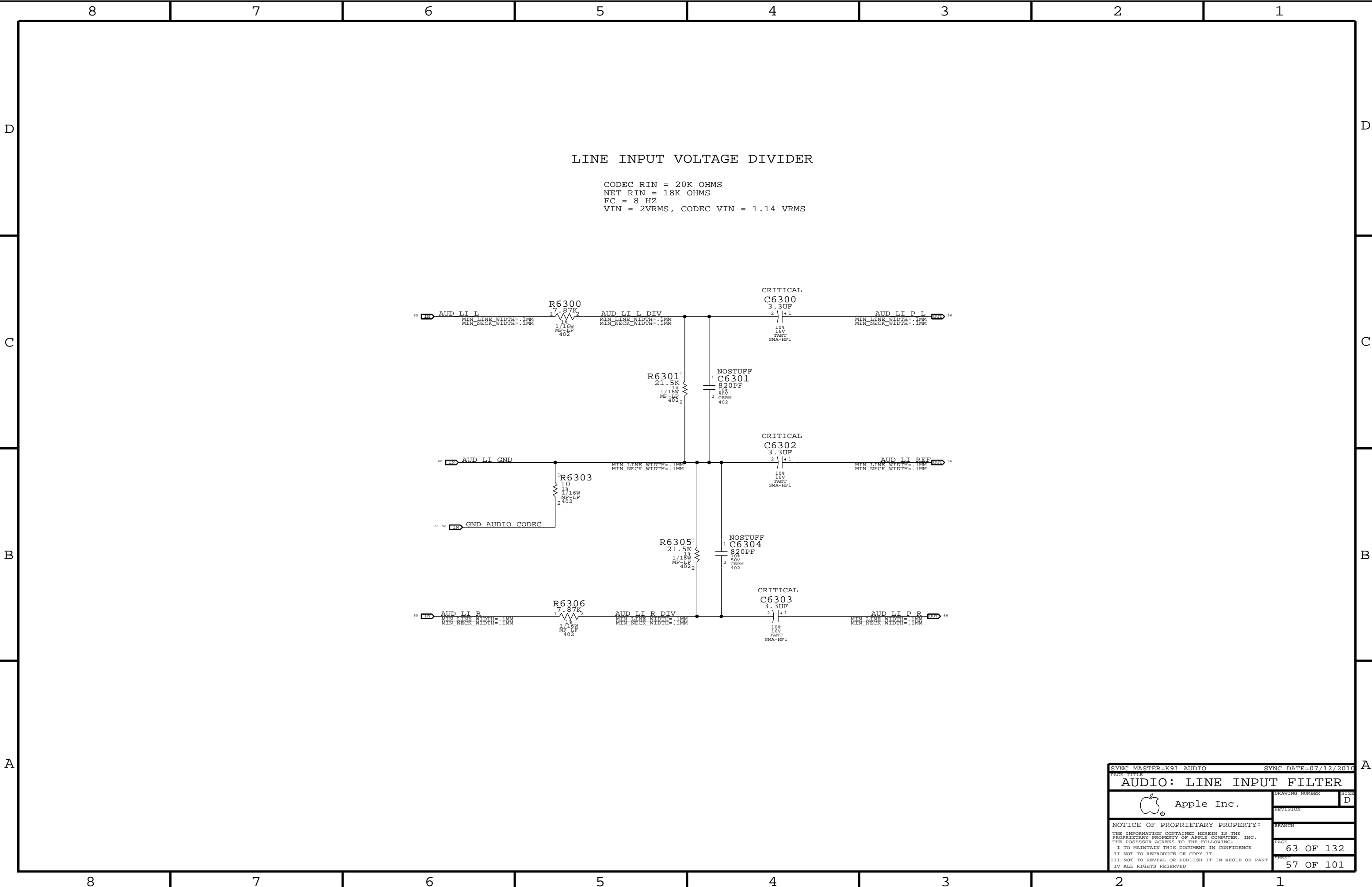


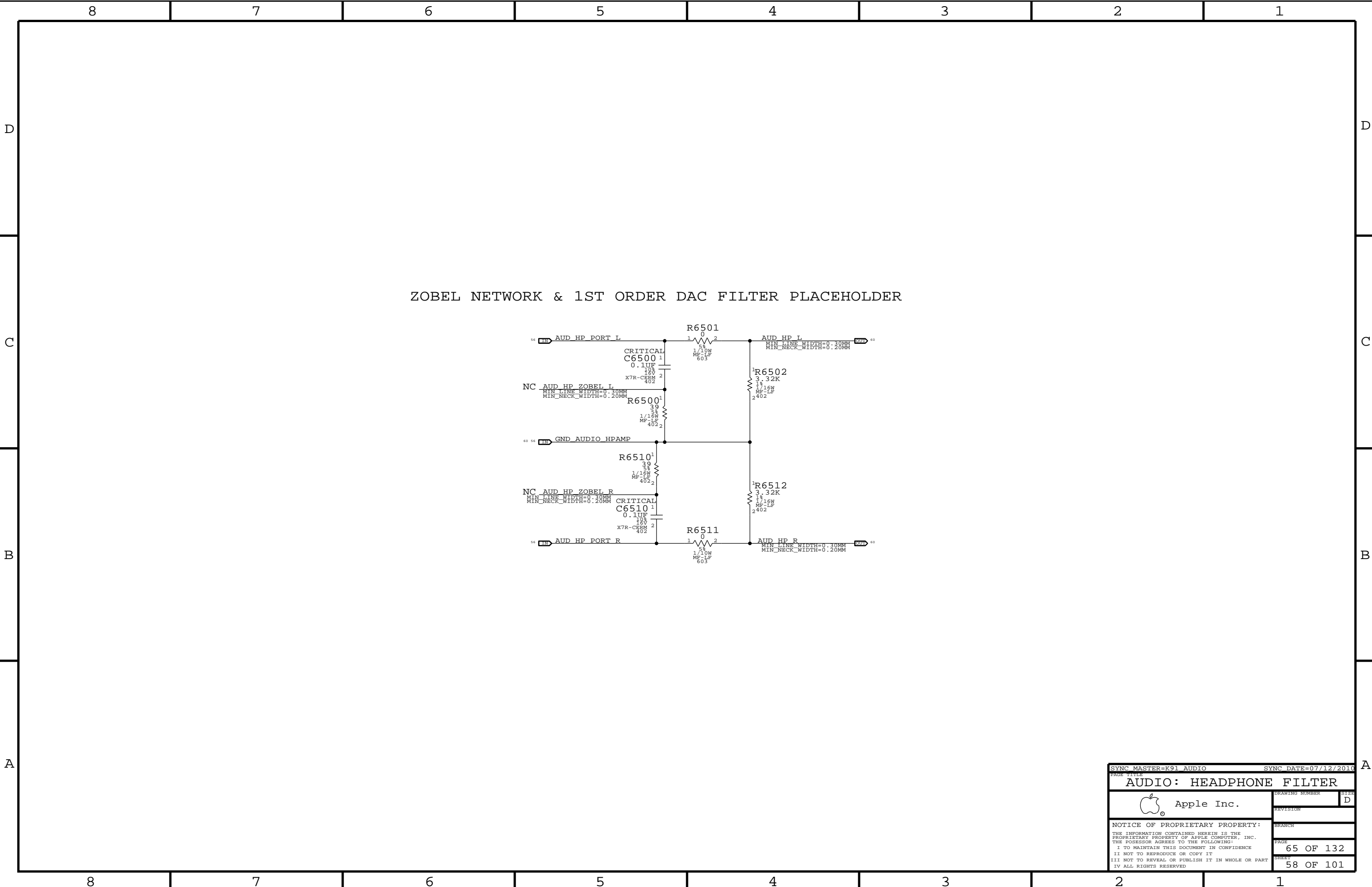


NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=K91 AUDIO		SYNC DATE=09/30/2010	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
 Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		62	OF 132
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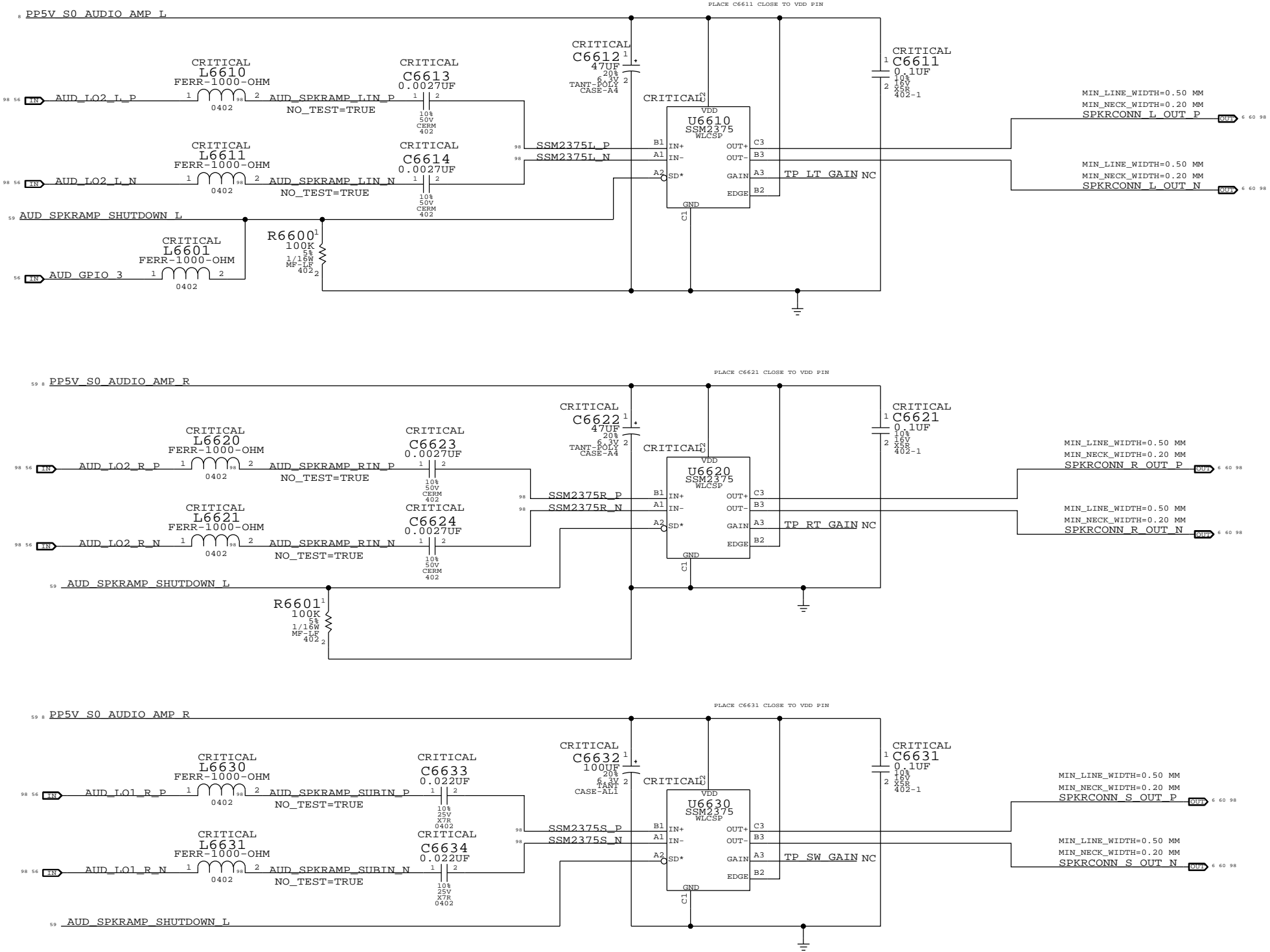





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A

3X MONO SPEAKER AMPLIFIERS (SSM2375)
APN: 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = ~737 HZ
1ST ORDER FC (SUB) = ~90 HZ

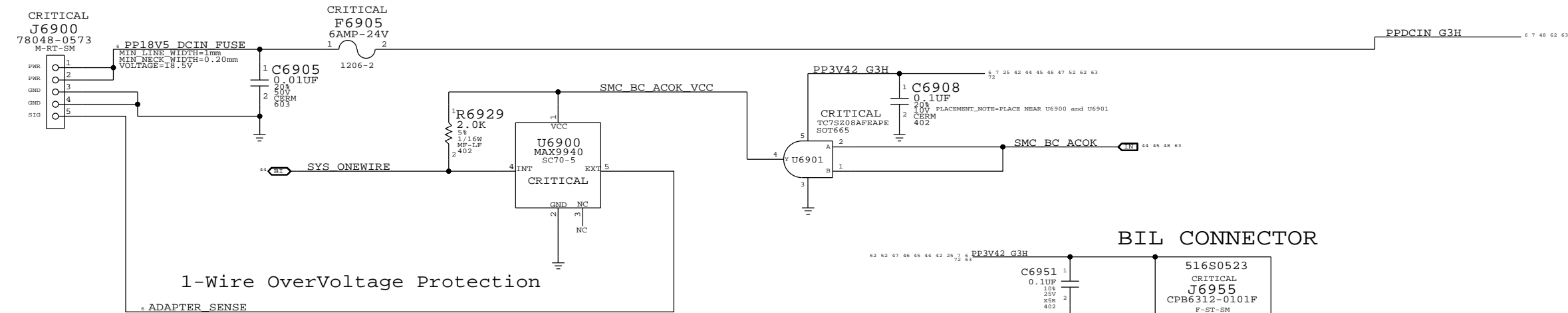


SYNC MASTER=K91 AUDIO		SYNC DATE=07/12/2010	
PAGE TITLE			
AUDIO: SPEAKER AMP			
 Apple Inc.		DRAWING NUMBER	SIZE
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		BRANCH	
		PAGE	66 OF 132
		SHEET	59 OF 101

8 7 6 5 4 3 2 1

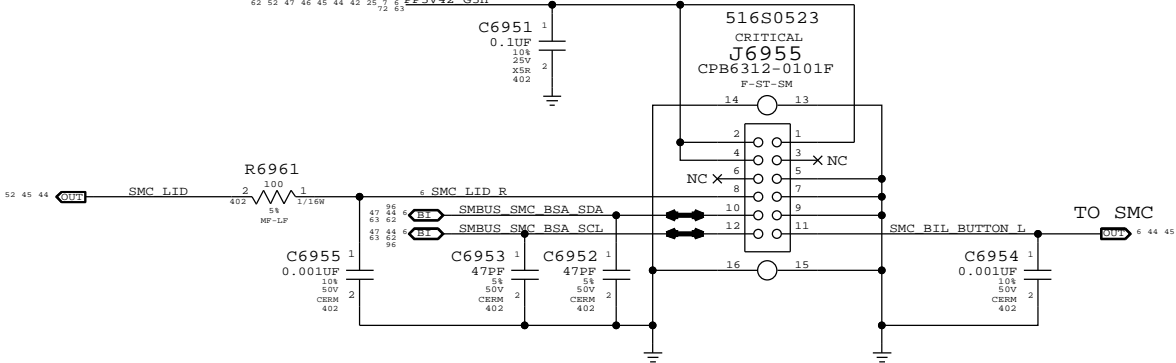
8 7 6 5 4 3 2 1

MagSafe DC Power Jack



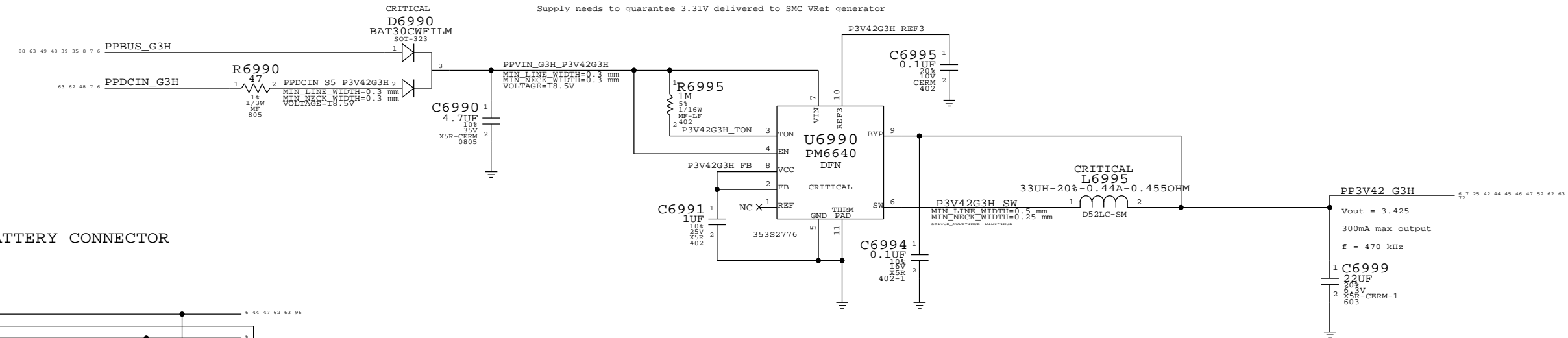
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR

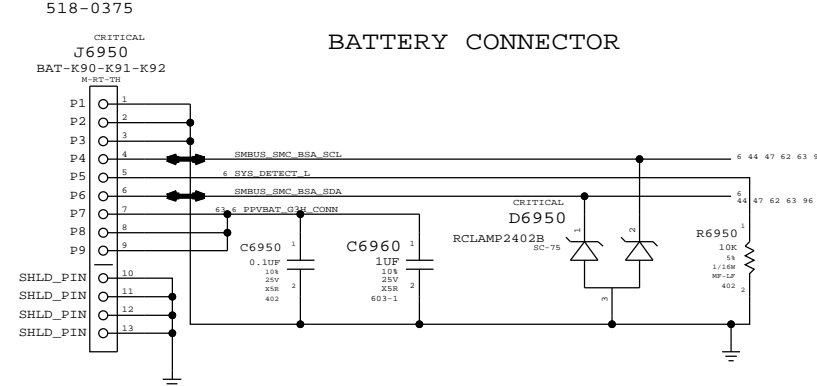


3.425V "G3Hot" Supply

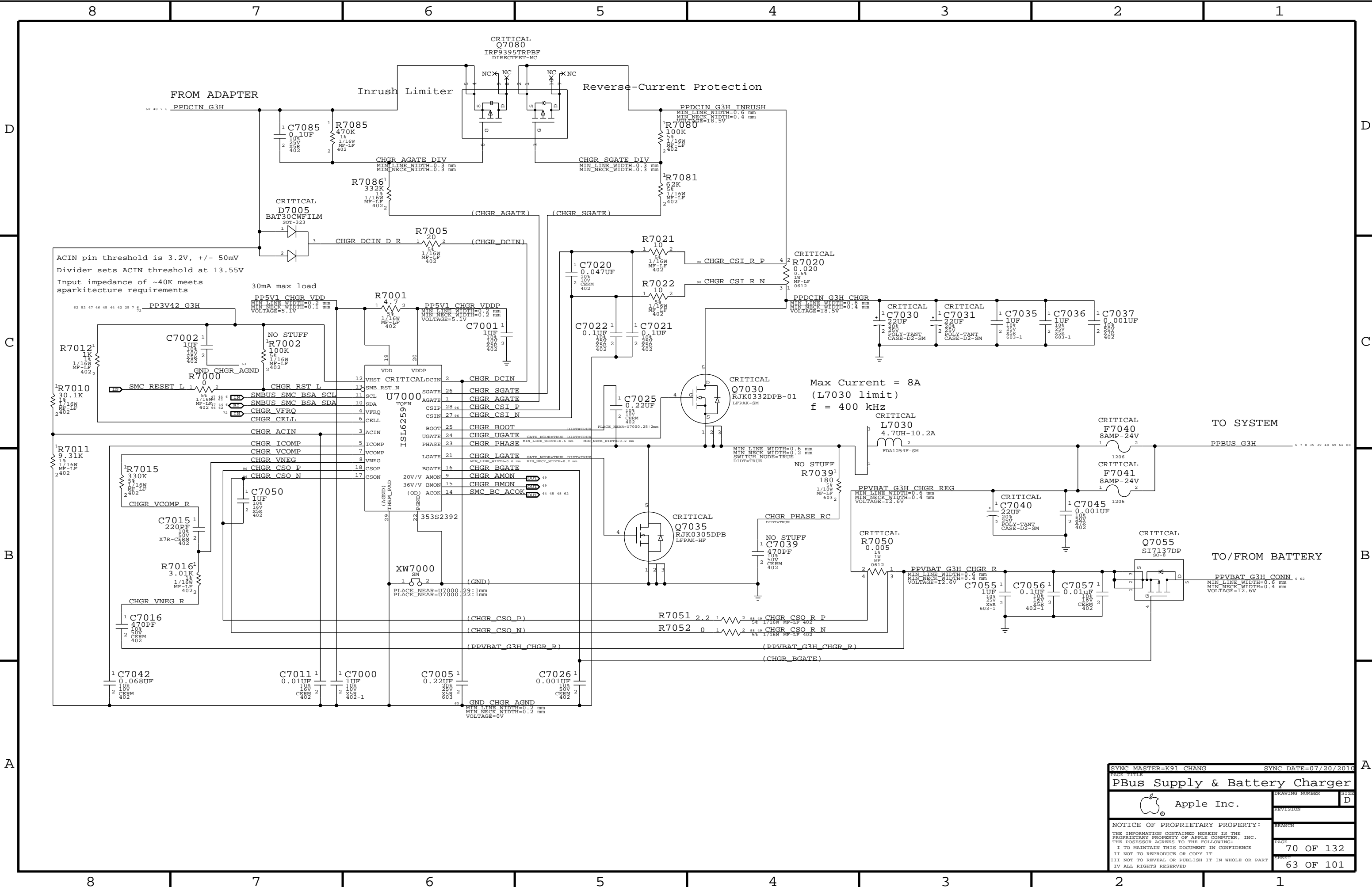
Supply needs to guarantee 3.31V delivered to SMC VRef generator

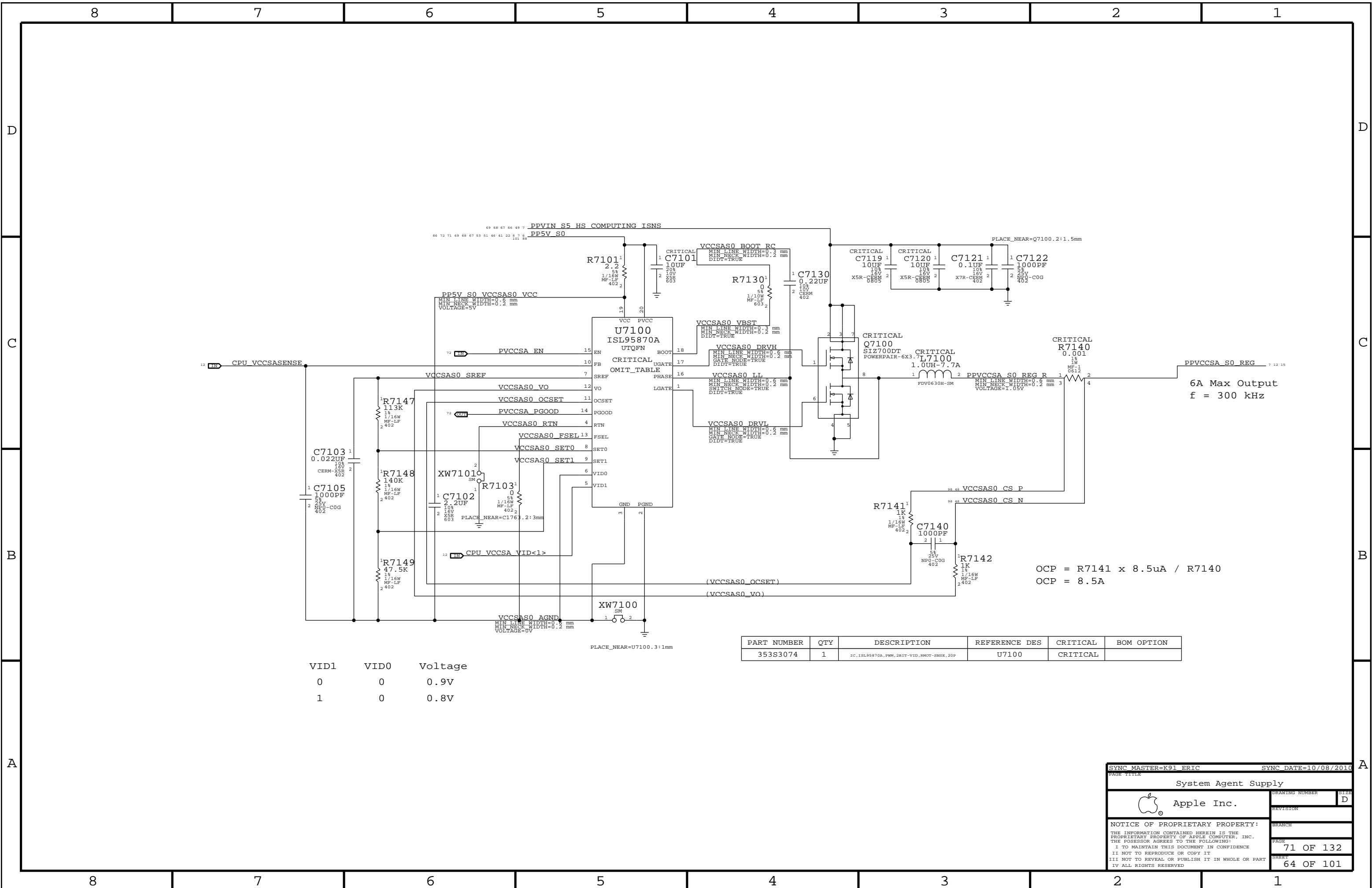


BATTERY CONNECTOR



PAGE TITLE		PAGE	
DC-In & Battery Connectors		69 OF 132	
Apple Inc.		62 OF 101	
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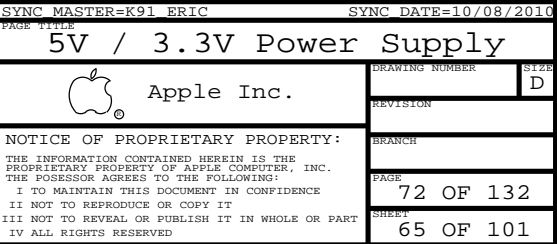
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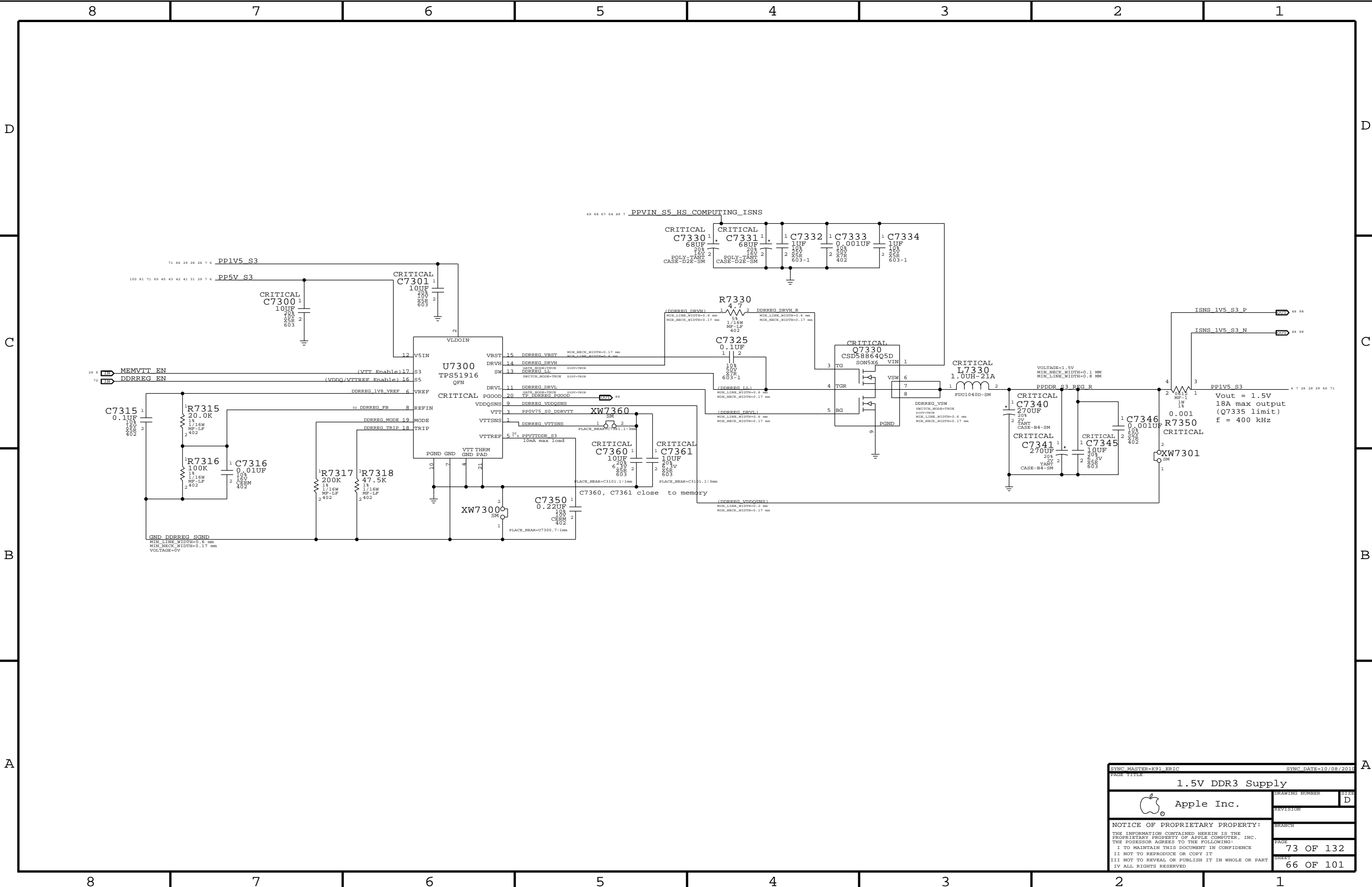
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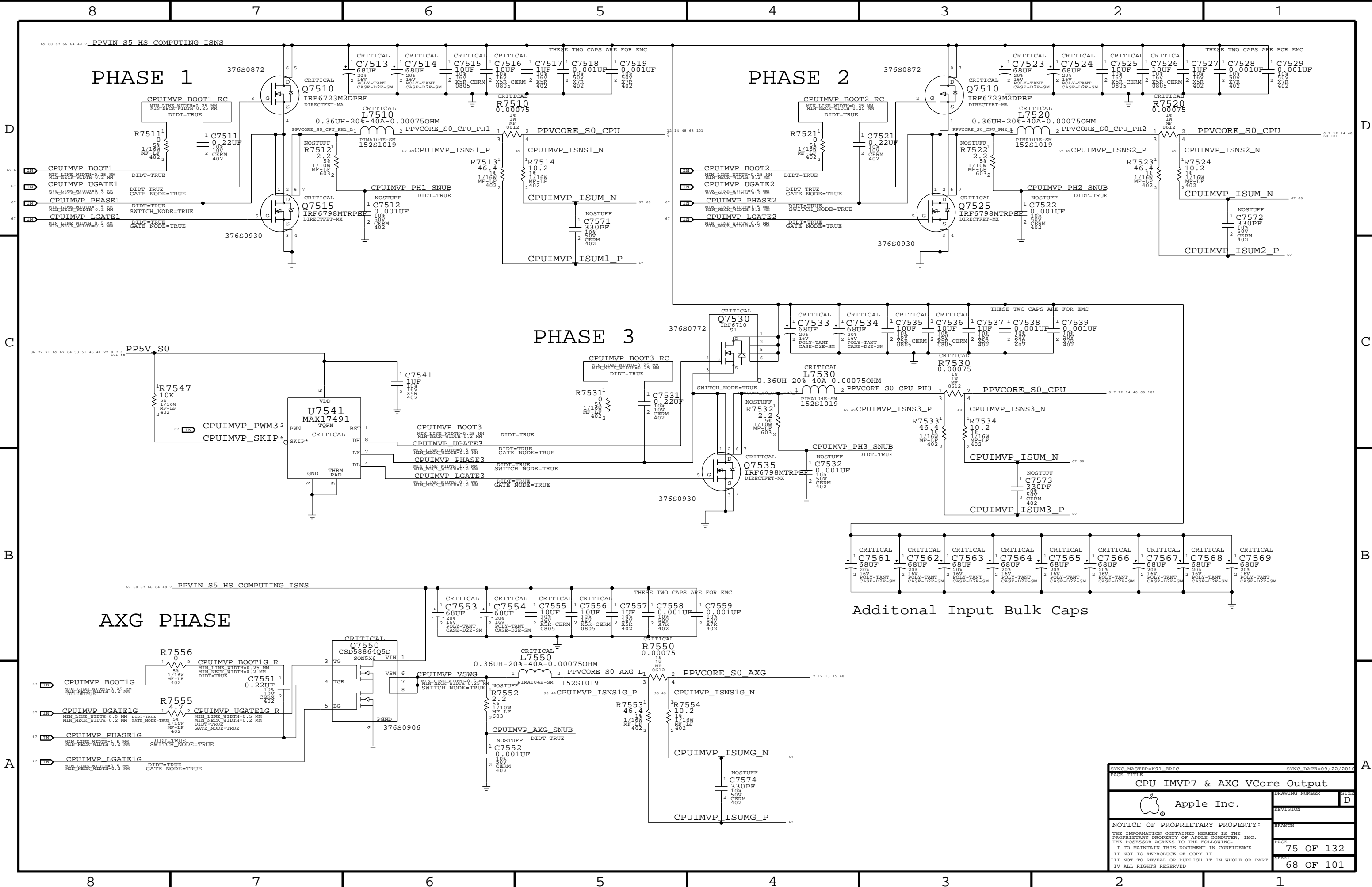
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SYNC MASTER=K91 ERIC		SYNC DATE=09/22/2010	
PAGE TITLE			
CPU IMVP7 & AXG VCore Output			
 Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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		PAGE	75 OF 132
		SHEET	68 OF 101

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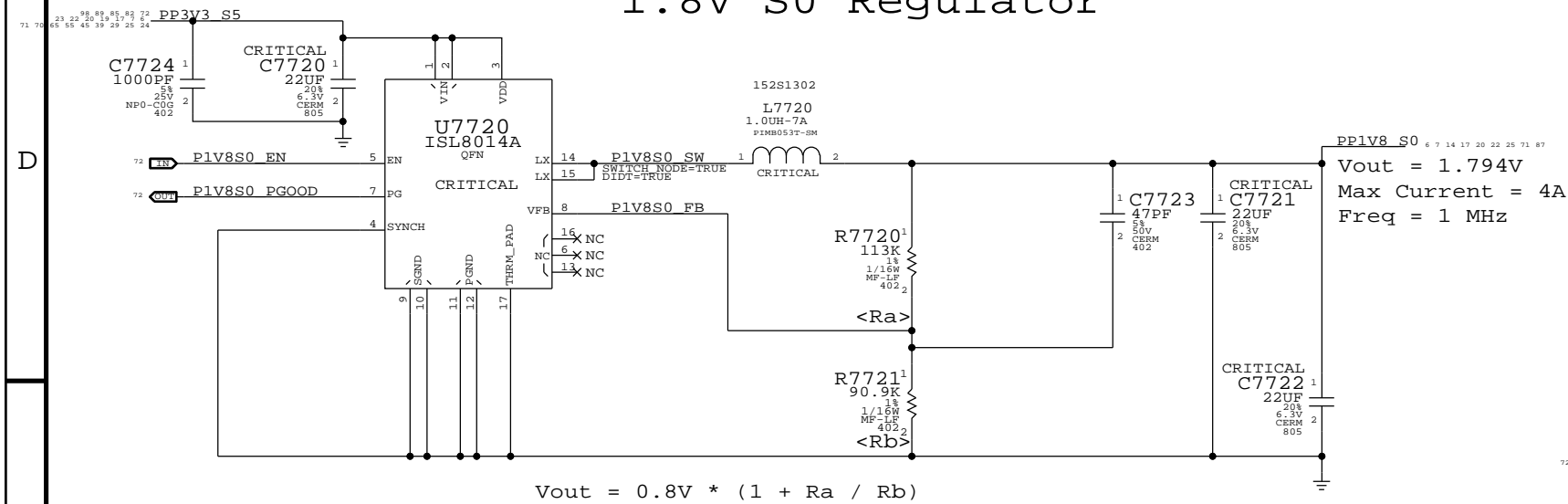
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C

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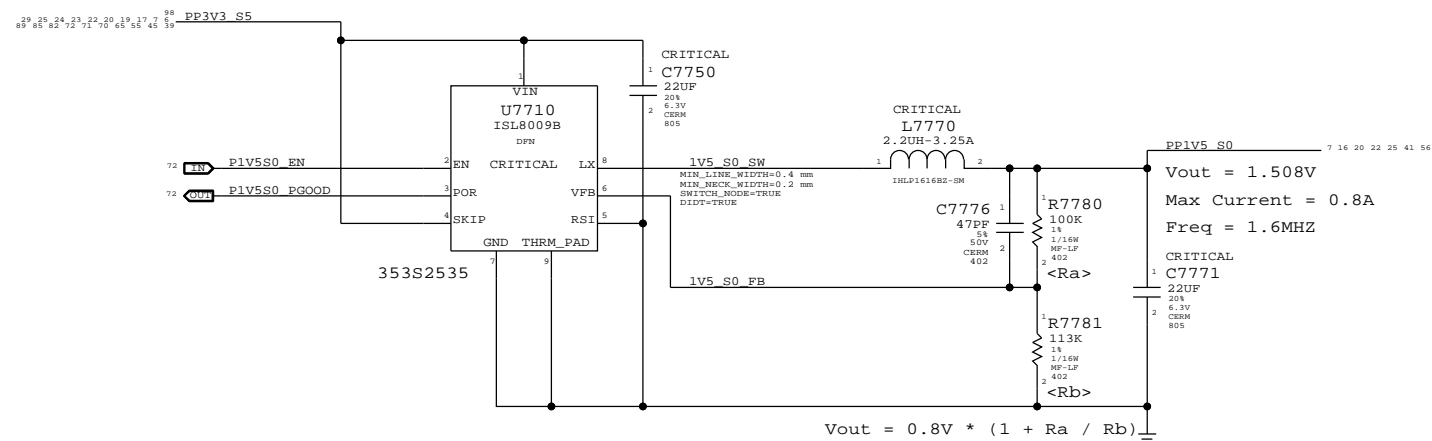
7

1.8V S0 Regulator



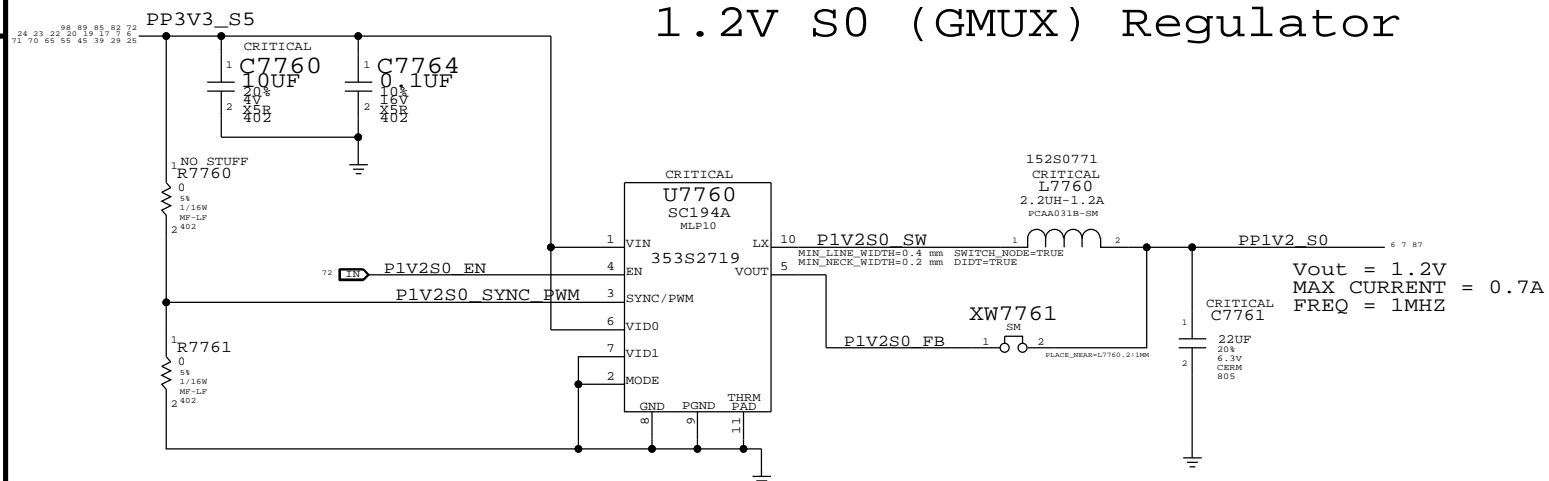
$$V_{out} = 0.8V * (1 + R_a / R_b)$$

1.5V S0 Regulator



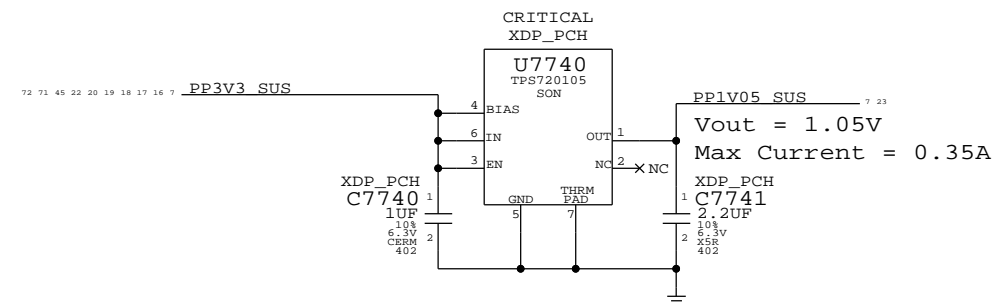
$$V_{out} = 0.8V * (1 + R_a / R_b)$$

1.2V S0 (GMUX) Regulator

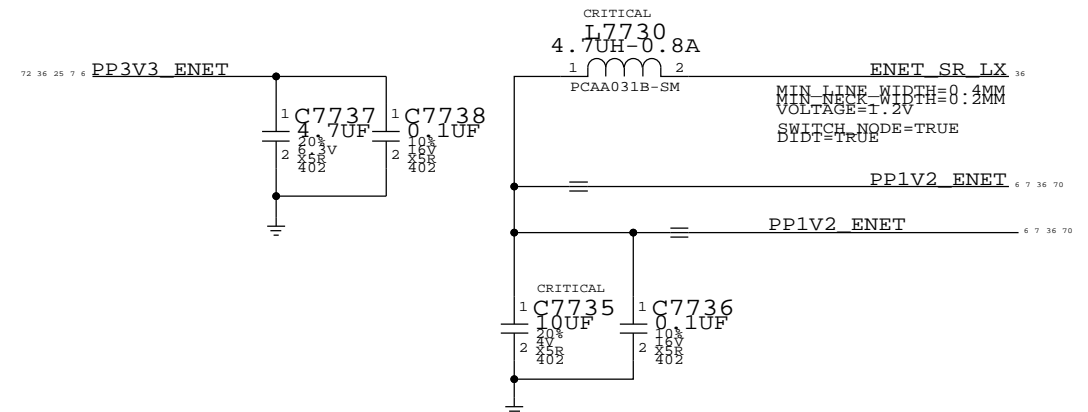



1.05V SUS LDO

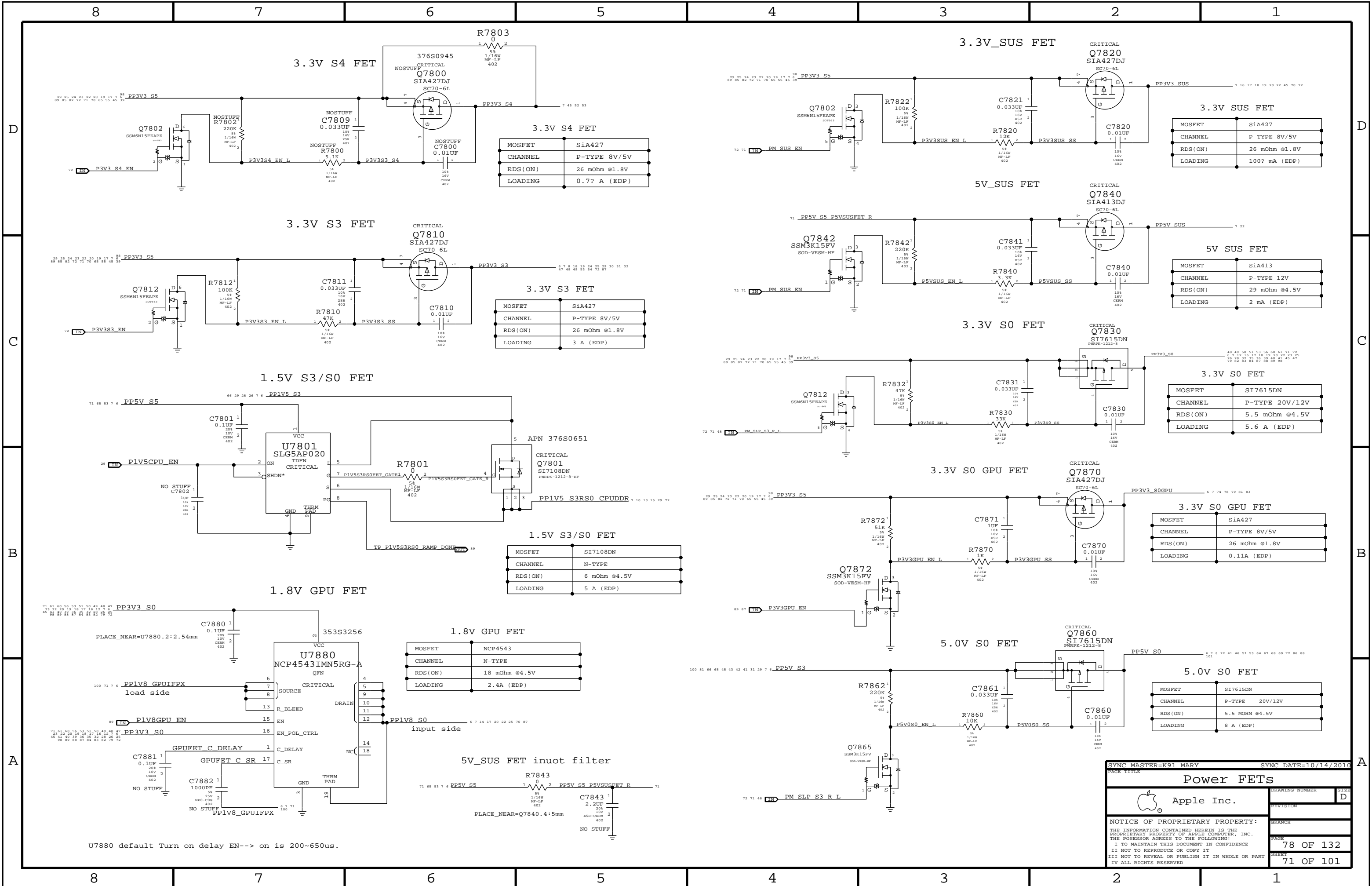
Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in Sus. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



CAESAR IV 1.2V INT.VR CMPTS



SYNCH MASTER=K91 ERIC		SYNCH DATE=11/01/2010	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.		DRAWING NUMBER	
		SIZE	
		D	
		REVISION	
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SYNC MASTER=K91 MARY

SYNC DATE=10/14/2010

Power FETs

Apple Inc.

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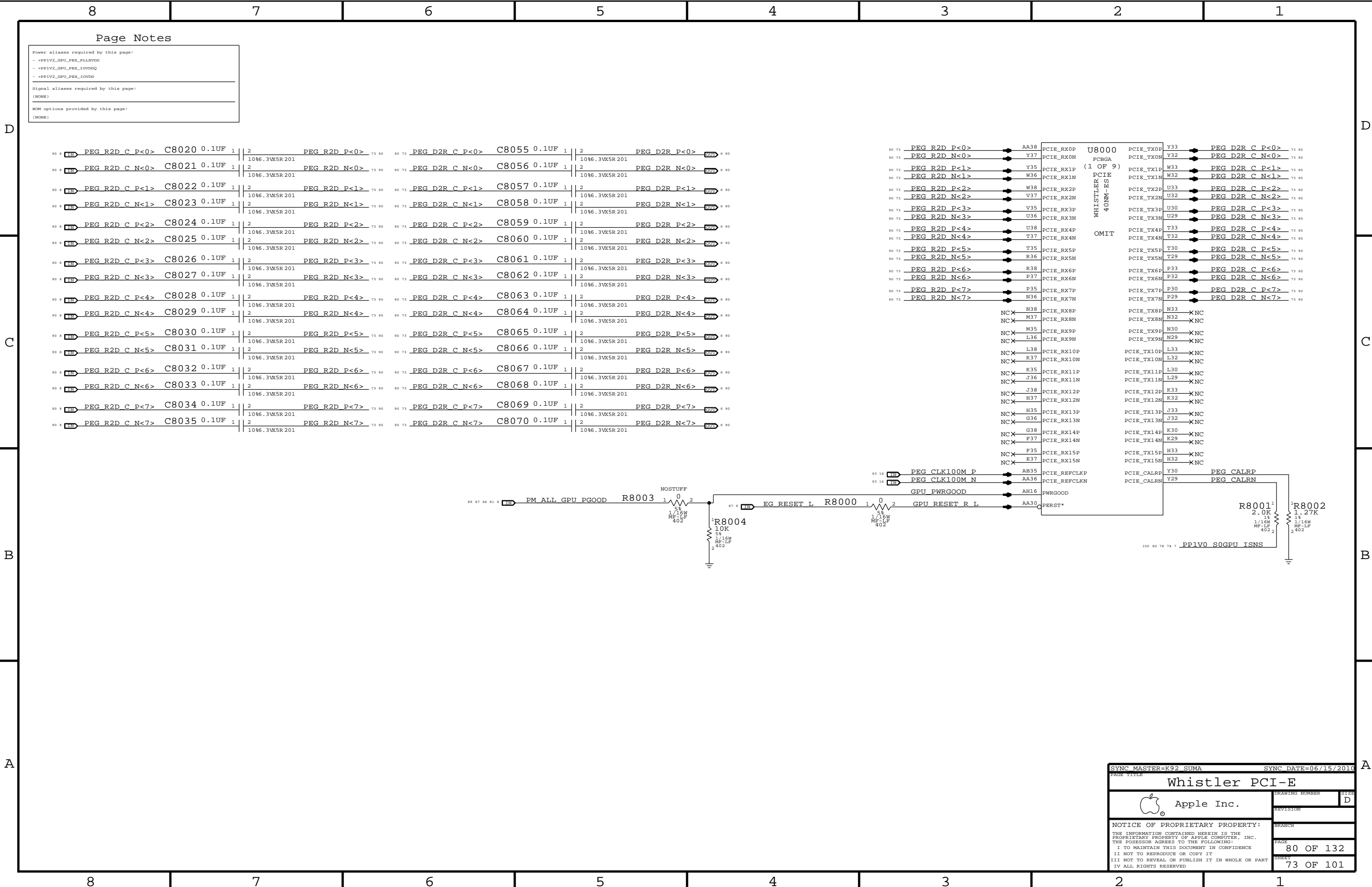
OF 132

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OF 101



Page Notes

Power aliases required by this page:

- =PP1V2_GPU_PEX_PLLEXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

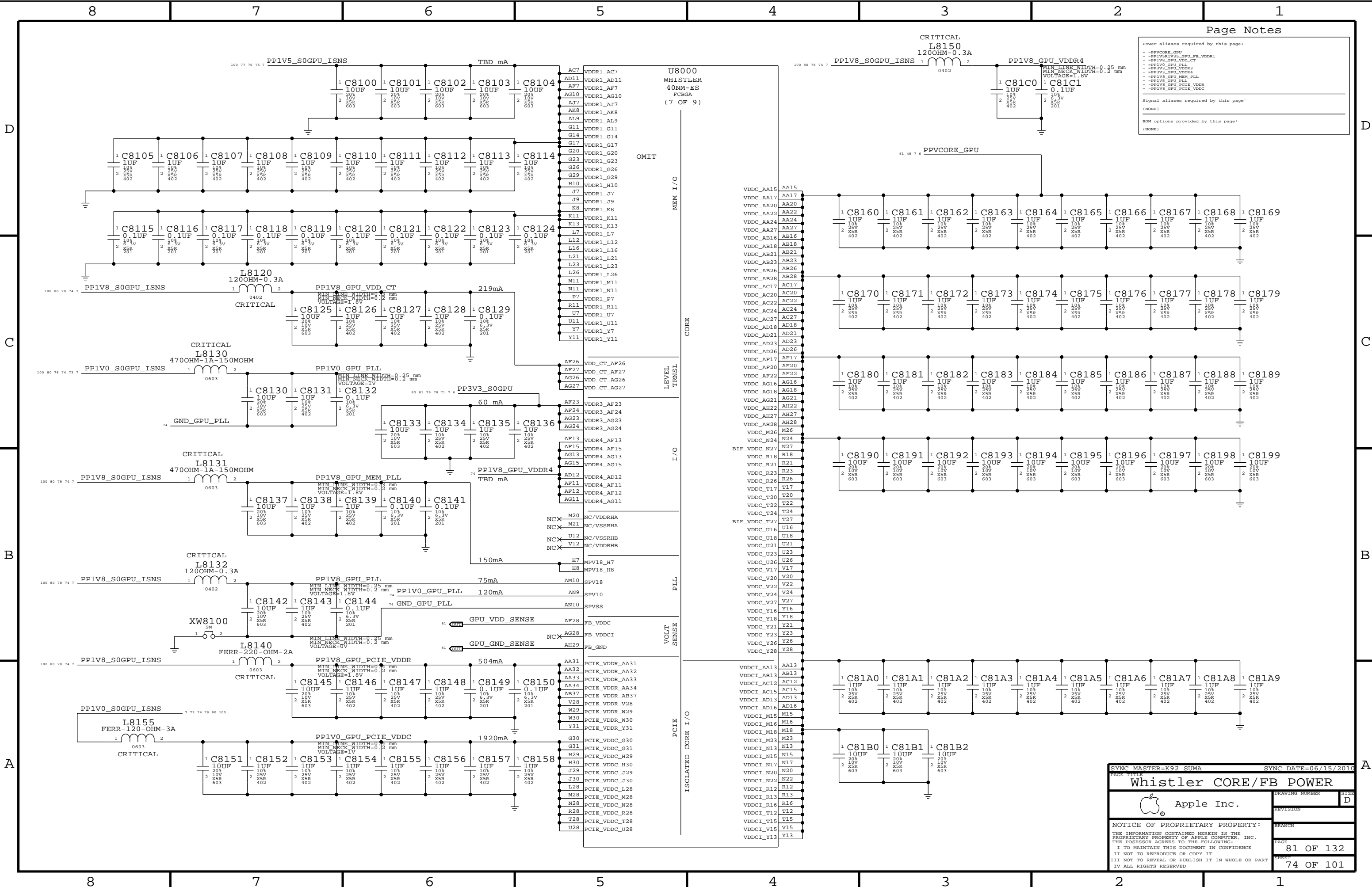
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

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90 73	PEG R2D N<0>	Y37	PCIE_RX0N	FCBGA	PCIE_TX0N	Y32	PEG D2R C N<0>	73 90
90 73	PEG R2D P<1>	Y35	PCIE_RX1P	(1 OF 9)	PCIE_TX1P	W33	PEG D2R C P<1>	73 90
90 73	PEG R2D N<1>	W36	PCIE_RX1N	PCIE	PCIE_TX1N	W32	PEG D2R C N<1>	73 90
90 73	PEG R2D P<2>	W38	PCIE_RX2P	WHISTLER	PCIE_TX2P	U33	PEG D2R C P<2>	73 90
90 73	PEG R2D N<2>	V37	PCIE_RX2N	40NM-ES	PCIE_TX2N	U32	PEG D2R C N<2>	73 90
90 73	PEG R2D P<3>	V35	PCIE_RX3P	OMIT	PCIE_TX3P	U30	PEG D2R C P<3>	73 90
90 73	PEG R2D N<3>	U36	PCIE_RX3N		PCIE_TX3N	U29	PEG D2R C N<3>	73 90
90 73	PEG R2D P<4>	U38	PCIE_RX4P		PCIE_TX4P	T33	PEG D2R C P<4>	73 90
90 73	PEG R2D N<4>	T37	PCIE_RX4N		PCIE_TX4N	T32	PEG D2R C N<4>	73 90
90 73	PEG R2D P<5>	T35	PCIE_RX5P		PCIE_TX5P	T30	PEG D2R C P<5>	73 90
90 73	PEG R2D N<5>	R36	PCIE_RX5N		PCIE_TX5N	T29	PEG D2R C N<5>	73 90
90 73	PEG R2D P<6>	R38	PCIE_RX6P		PCIE_TX6P	P33	PEG D2R C P<6>	73 90
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90 73	PEG R2D N<7>	N36	PCIE_RX7N		PCIE_TX7N	P29	PEG D2R C N<7>	73 90
		NCX	N38	PCIE_RX8P	PCIE_TX8P	N33	XNC	
		NCX	M37	PCIE_RX8N	PCIE_TX8N	N32	XNC	
		NCX	M35	PCIE_RX9P	PCIE_TX9P	N30	XNC	
		NCX	L36	PCIE_RX9N	PCIE_TX9N	N29	XNC	
		NCX	L38	PCIE_RX10P	PCIE_TX10P	L33	XNC	
		NCX	K37	PCIE_RX10N	PCIE_TX10N	L32	XNC	
		NCX	K35	PCIE_RX11P	PCIE_TX11P	L30	XNC	
		NCX	J36	PCIE_RX11N	PCIE_TX11N	L29	XNC	
		NCX	J38	PCIE_RX12P	PCIE_TX12P	K33	XNC	
		NCX	H37	PCIE_RX12N	PCIE_TX12N	K32	XNC	
		NCX	H35	PCIE_RX13P	PCIE_TX13P	J33	XNC	
		NCX	G36	PCIE_RX13N	PCIE_TX13N	J32	XNC	
		NCX	G38	PCIE_RX14P	PCIE_TX14P	K30	XNC	
		NCX	F37	PCIE_RX14N	PCIE_TX14N	K29	XNC	
		NCX	F35	PCIE_RX15P	PCIE_TX15P	H33	XNC	
		NCX	E37	PCIE_RX15N	PCIE_TX15N	H32	XNC	
93 16	PEG CLK100M P	AB35	PCIE_REFCLKP		PCIE_CALRP	Y30	PEG CALRP	
93 16	PEG CLK100M N	AA36	PCIE_REFCLKN		PCIE_CALRN	Y29	PEG CALRN	
	GPU PWRGOOD	AH16	PWRGOOD					
	GPU RESET R L	AA30	PERST*					



Page Notes

Power aliases required by this page:

-

PPVCORE_GPU

-

PP1V8S1V15_GPU_FB_VDDCR1

-

PP1V8_GPU_VDD_CT

-

PP1V0_GPU_PLL

-

PP3V3_GPU_VDDCR3

-

PP3V3_GPU_VDDCR4

-

PP1V8_GPU_MEM_PLL

-

PP1V8_GPU_PLL

-

PP1V8_GPU_PCIE_VDDCR

-

PP1V8_GPU_PCIE_VDDCR

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC MASTER=K92_SUMA

SYNC DATE=06/15/2010

Whistler CORE/FB POWER

Apple Inc.

Apple logo

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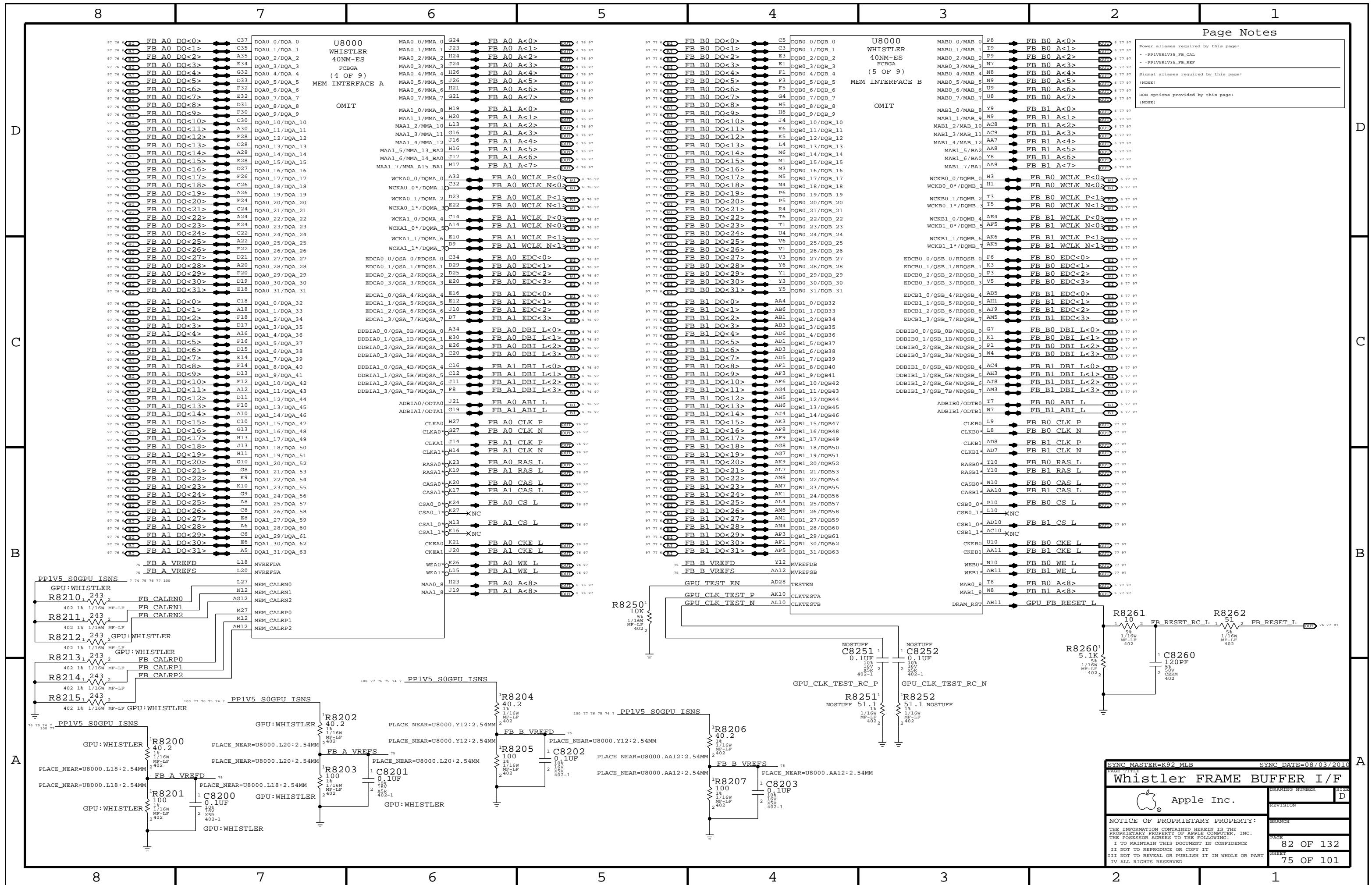
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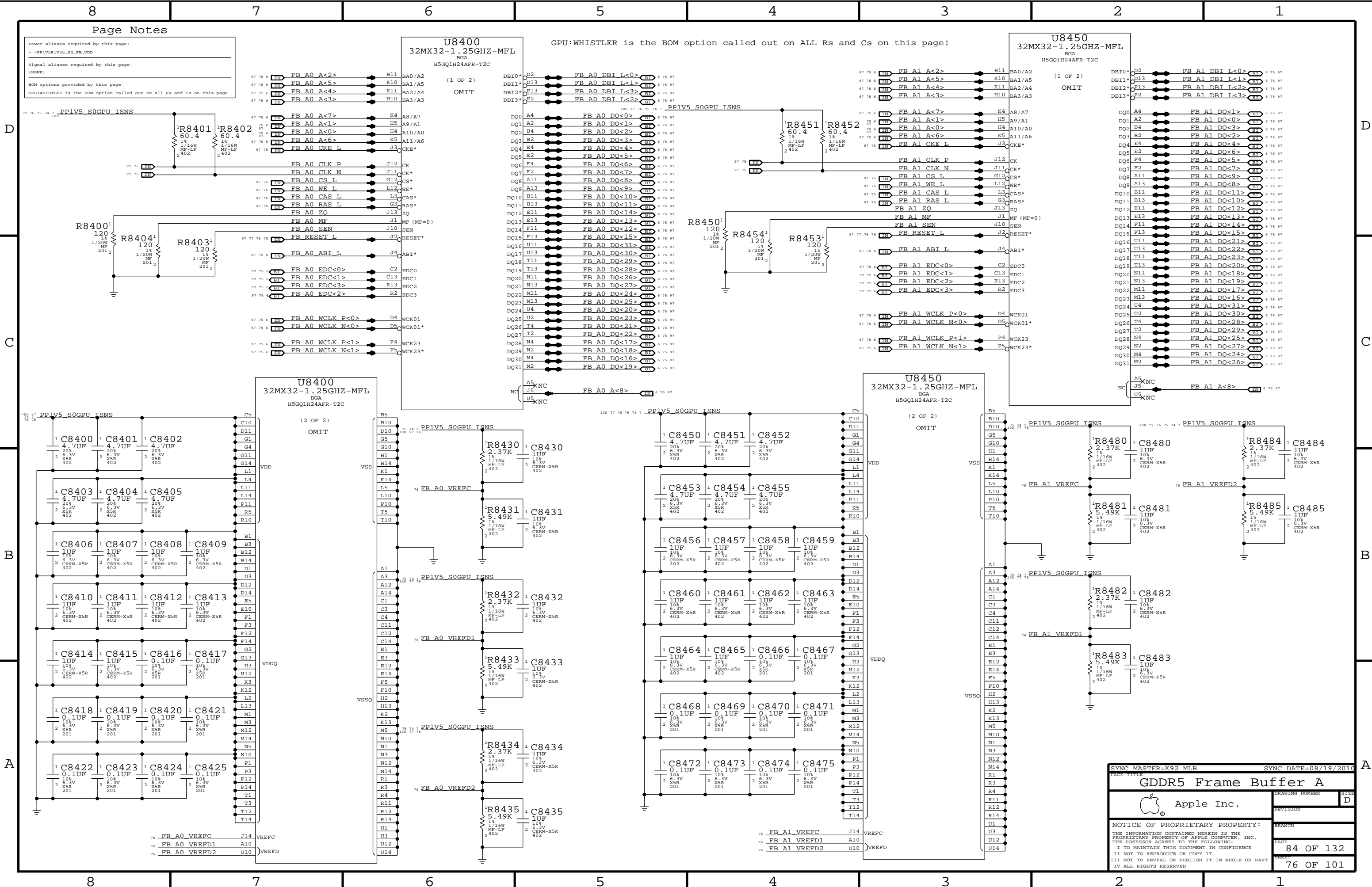
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Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
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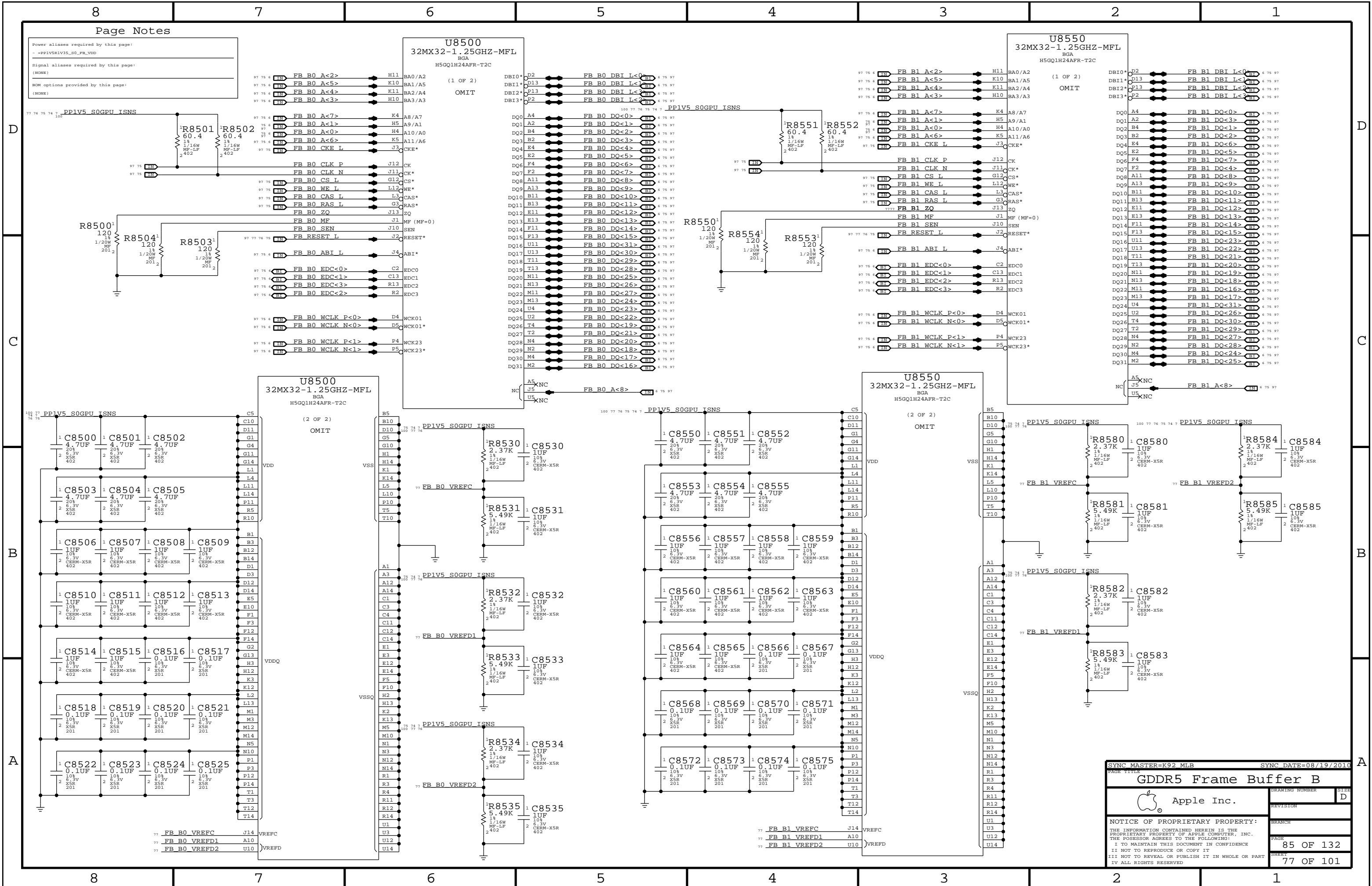
BOM options provided by this page:
GPU:WHISTLER is the BOM option called out on all Rs and Cs on this page

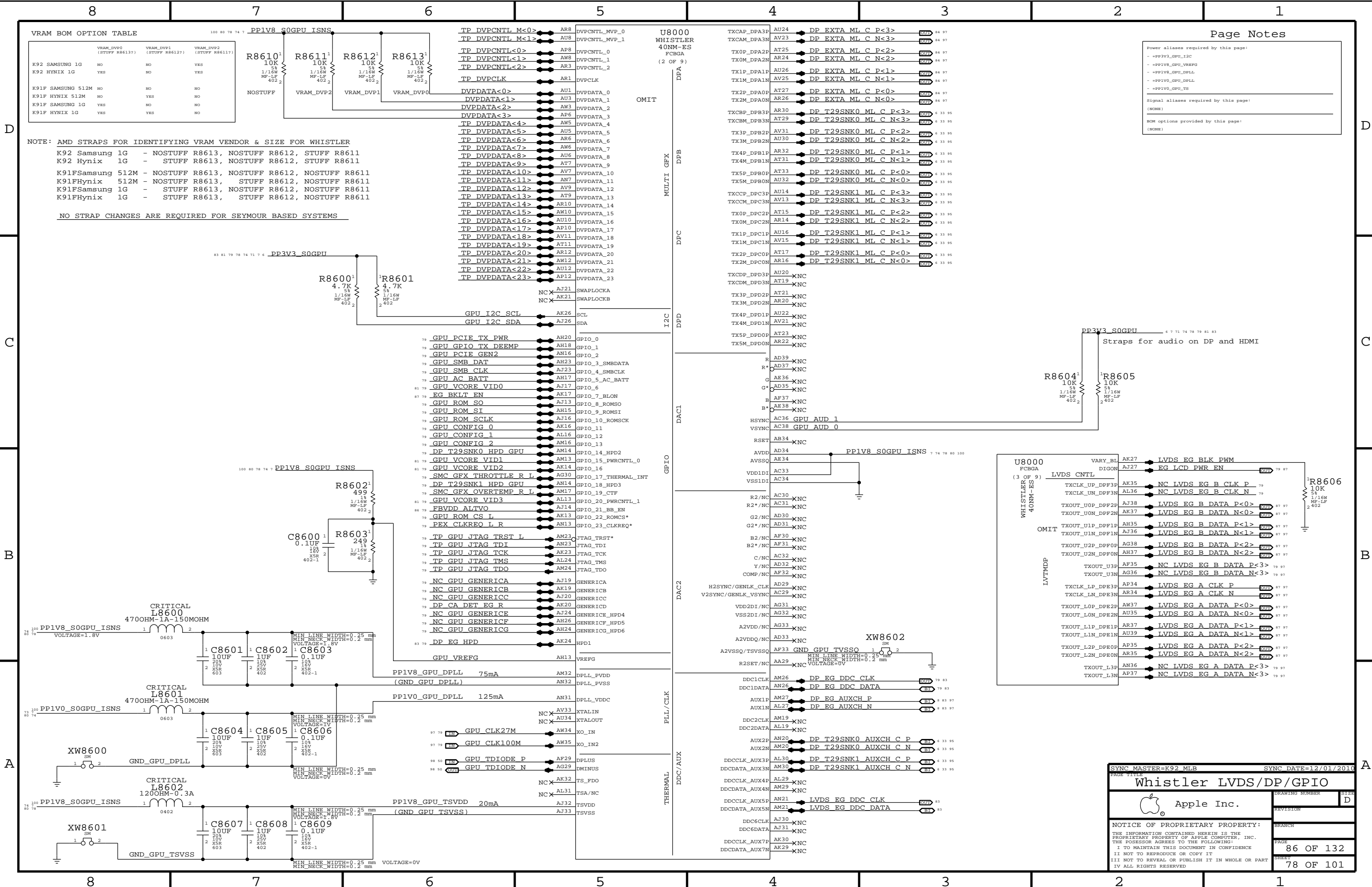
U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

GPU:WHISTLER is the BOM option called out on ALL Rs and Cs on this page!

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

SYNC MASTER=K92_MLB		SYNC DATE=08/19/2010	
GDDR5 Frame Buffer A			
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VRAM BOM OPTION TABLE

	VRAM_DVP0 (STUFF R8613?)	VRAM_DVP1 (STUFF R8612?)	VRAM_DVP2 (STUFF R8611?)
K92 SAMSUNG 1G	NO	NO	YES
K92 HYNIX 1G	YES	NO	YES
K91F SAMSUNG 512M	NO	NO	NO
K91F HYNIX 512M	NO	YES	NO
K91F SAMSUNG 1G	YES	NO	NO
K91F HYNIX 1G	YES	YES	NO

NOTE: AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

K91FSamsung 512M - NOSTUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 512M - NOSTUFF R8613, STUFF R8612, NOSTUFF R8611
K91FSamsung 1G - STUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 1G - STUFF R8613, STUFF R8612, NOSTUFF R8611

NO STRAP CHANGES ARE REQUIRED FOR SEYMOUR BASED SYSTEMS

Page Notes

Power aliases required by this page:

- PP3V3_GPU_I2C
- PP1V8_GPU_VREF
- PP1V8_GPU_DPLL
- PP1V0_GPU_DPLL
- PP1V0_GPU_TS

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC MASTER=K92 MLB SYNC DATE=12/01/2010

Whistler LVDS/DP/GPIO

Apple Inc.

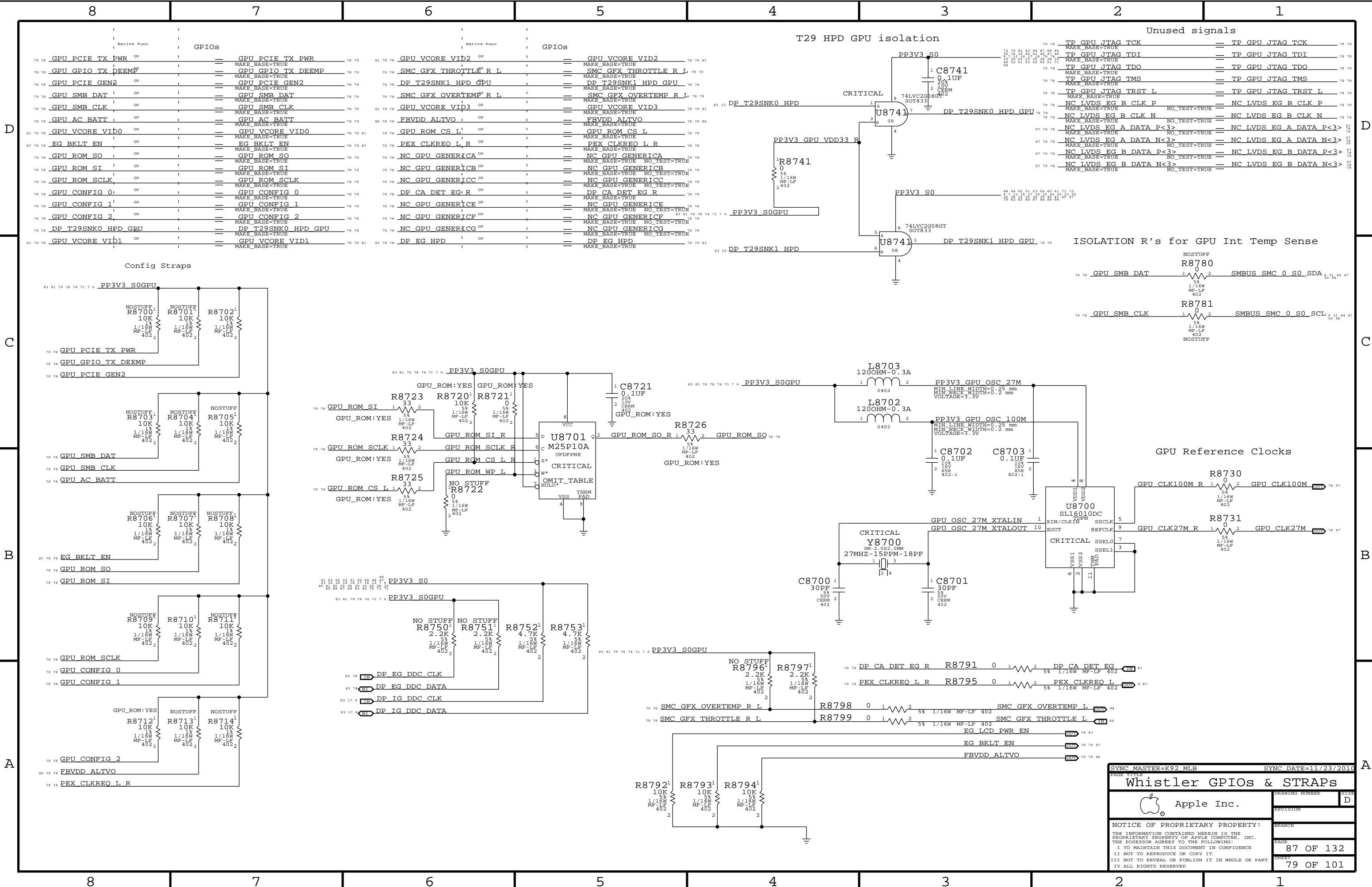
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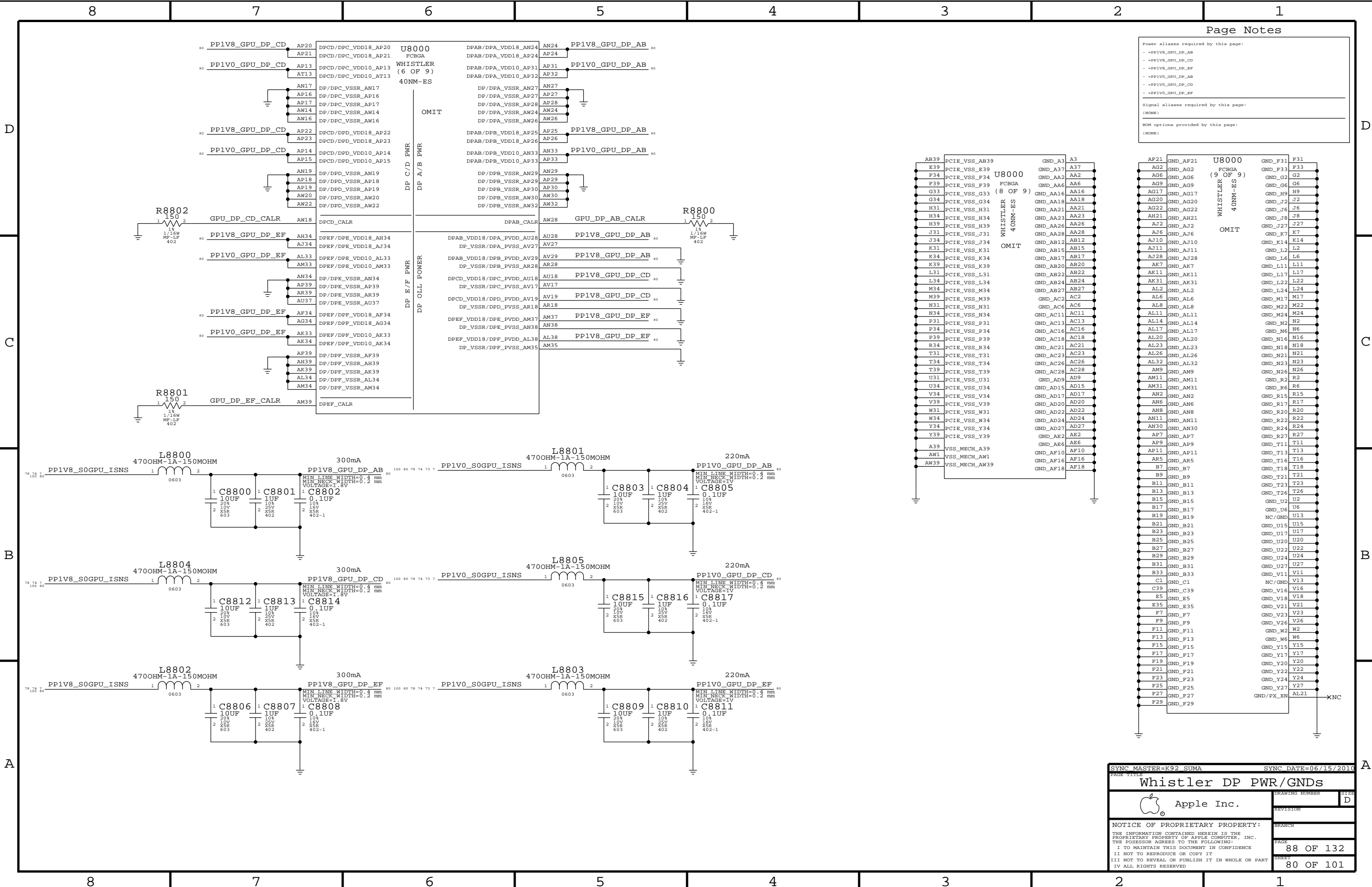
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Power aliases required by this page:	
- PP1V8_GPU_DP_AB	
- PP1V8_GPU_DP_CD	
- PP1V8_GPU_DP_EF	
- PP1V0_GPU_DP_AB	
- PP1V0_GPU_DP_CD	
- PP1V0_GPU_DP_EF	
Signal aliases required by this page:	
(NONE)	
BOM options provided by this page:	
(NONE)	

AB39	PCIE_VSS_AB39	GND_A3	A3
E39	PCIE_VSS_E39	GND_A37	A37
F34	PCIE_VSS_F34	GND_AA2	AA2
F39	PCIE_VSS_F39	GND_AA6	AA6
G33	PCIE_VSS_G33	GND_AA16	AA16
G34	PCIE_VSS_G34	GND_AA18	AA18
H31	PCIE_VSS_H31	GND_AA21	AA21
H34	PCIE_VSS_H34	GND_AA23	AA23
H39	PCIE_VSS_H39	GND_AA26	AA26
J31	PCIE_VSS_J31	GND_AA28	AA28
J34	PCIE_VSS_J34	GND_AB12	AB12
K31	PCIE_VSS_K31	GND_AB15	AB15
K34	PCIE_VSS_K34	GND_AB17	AB17
K39	PCIE_VSS_K39	GND_AB20	AB20
L31	PCIE_VSS_L31	GND_AB22	AB22
L34	PCIE_VSS_L34	GND_AB24	AB24
M34	PCIE_VSS_M34	GND_AB27	AB27
M39	PCIE_VSS_M39	GND_AC2	AC2
N31	PCIE_VSS_N31	GND_AC6	AC6
N34	PCIE_VSS_N34	GND_AC11	AC11
P31	PCIE_VSS_P31	GND_AC13	AC13
P34	PCIE_VSS_P34	GND_AC16	AC16
P39	PCIE_VSS_P39	GND_AC18	AC18
R34	PCIE_VSS_R34	GND_AC21	AC21
T31	PCIE_VSS_T31	GND_AC23	AC23
T34	PCIE_VSS_T34	GND_AC26	AC26
T39	PCIE_VSS_T39	GND_AC28	AC28
U31	PCIE_VSS_U31	GND_AD9	AD9
U34	PCIE_VSS_U34	GND_AD15	AD15
V34	PCIE_VSS_V34	GND_AD17	AD17
V39	PCIE_VSS_V39	GND_AD20	AD20
W31	PCIE_VSS_W31	GND_AD22	AD22
W34	PCIE_VSS_W34	GND_AD24	AD24
Y34	PCIE_VSS_Y34	GND_AD27	AD27
Y39	PCIE_VSS_Y39	GND_AE2	AE2
A39	VSS_MECH_A39	GND_AE6	AE6
AW1	VSS_MECH_AW1	GND_AF10	AF10
AW39	VSS_MECH_AW39	GND_AF16	AF16
		GND_AF18	AF18

AF21	GND_AF21	U8000	GND_F31	F31
AG2	GND_AG2	(9 OF 9)	GND_F33	F33
AG6	GND_AG6	WHISTLER	GND_G2	G2
AG9	GND_AG9	40NM-ES	GND_G6	G6
AG17	GND_AG17	OMIT	GND_H9	H9
AG20	GND_AG20		GND_J2	J2
AG22	GND_AG22		GND_J6	J6
AH21	GND_AH21		GND_J8	J8
AJ2	GND_AJ2		GND_J27	J27
AJ6	GND_AJ6		GND_K7	K7
AJ10	GND_AJ10		GND_K14	K14
AJ11	GND_AJ11		GND_L2	L2
AJ28	GND_AJ28		GND_L6	L6
AK7	GND_AK7		GND_L11	L11
AK11	GND_AK11		GND_L17	L17
AK31	GND_AK31		GND_L22	L22
AL2	GND_AL2		GND_L24	L24
AL6	GND_AL6		GND_M17	M17
AL8	GND_AL8		GND_M22	M22
AL11	GND_AL11		GND_M24	M24
AL14	GND_AL14		GND_N2	N2
AL17	GND_AL17		GND_N6	N6
AL20	GND_AL20		GND_N16	N16
AL23	GND_AL23		GND_N18	N18
AL26	GND_AL26		GND_N21	N21
AL32	GND_AL32		GND_N23	N23
AM9	GND_AM9		GND_N26	N26
AM11	GND_AM11		GND_R2	R2
AM31	GND_AM31		GND_R6	R6
AN2	GND_AN2		GND_R15	R15
AN6	GND_AN6		GND_R17	R17
AN8	GND_AN8		GND_R20	R20
AN11	GND_AN11		GND_R22	R22
AN30	GND_AN30		GND_R24	R24
AP7	GND_AP7		GND_R27	R27
AP9	GND_AP9		GND_T11	T11
AP11	GND_AP11		GND_T13	T13
AR5	GND_AR5		GND_T16	T16
B7	GND_B7		GND_T18	T18
B9	GND_B9		GND_T21	T21
B11	GND_B11		GND_T23	T23
B13	GND_B13		GND_T26	T26
B15	GND_B15		GND_U2	U2
B17	GND_B17		GND_U6	U6
B19	GND_B19		NC/GND	U13
B21	GND_B21		GND_U15	U15
B23	GND_B23		GND_U17	U17
B25	GND_B25		GND_U20	U20
B27	GND_B27		GND_U22	U22
B29	GND_B29		GND_U24	U24
B31	GND_B31		GND_U27	U27
B33	GND_B33		GND_V11	V11
C1	GND_C1		NC/GND	V13
C39	GND_C39		GND_V16	V16
E5	GND_E5		GND_V18	V18
E35	GND_E35		GND_V21	V21
F7	GND_F7		GND_V23	V23
F9	GND_F9		GND_V26	V26
F11	GND_F11		GND_W2	W2
F13	GND_F13		GND_W6	W6
F15	GND_F15		GND_Y15	Y15
F17	GND_F17		GND_Y17	Y17
F19	GND_F19		GND_Y20	Y20
F21	GND_F21		GND_Y22	Y22
F23	GND_F23		GND_Y24	Y24
F25	GND_F25		GND_Y27	Y27
F27	GND_F27		GND/PX_EN	AL21
F29	GND_F29			

SYNC MASTER=K92 SUMA

SYNC DATE=06/15/2010

Whistler DP PWR/GNDs

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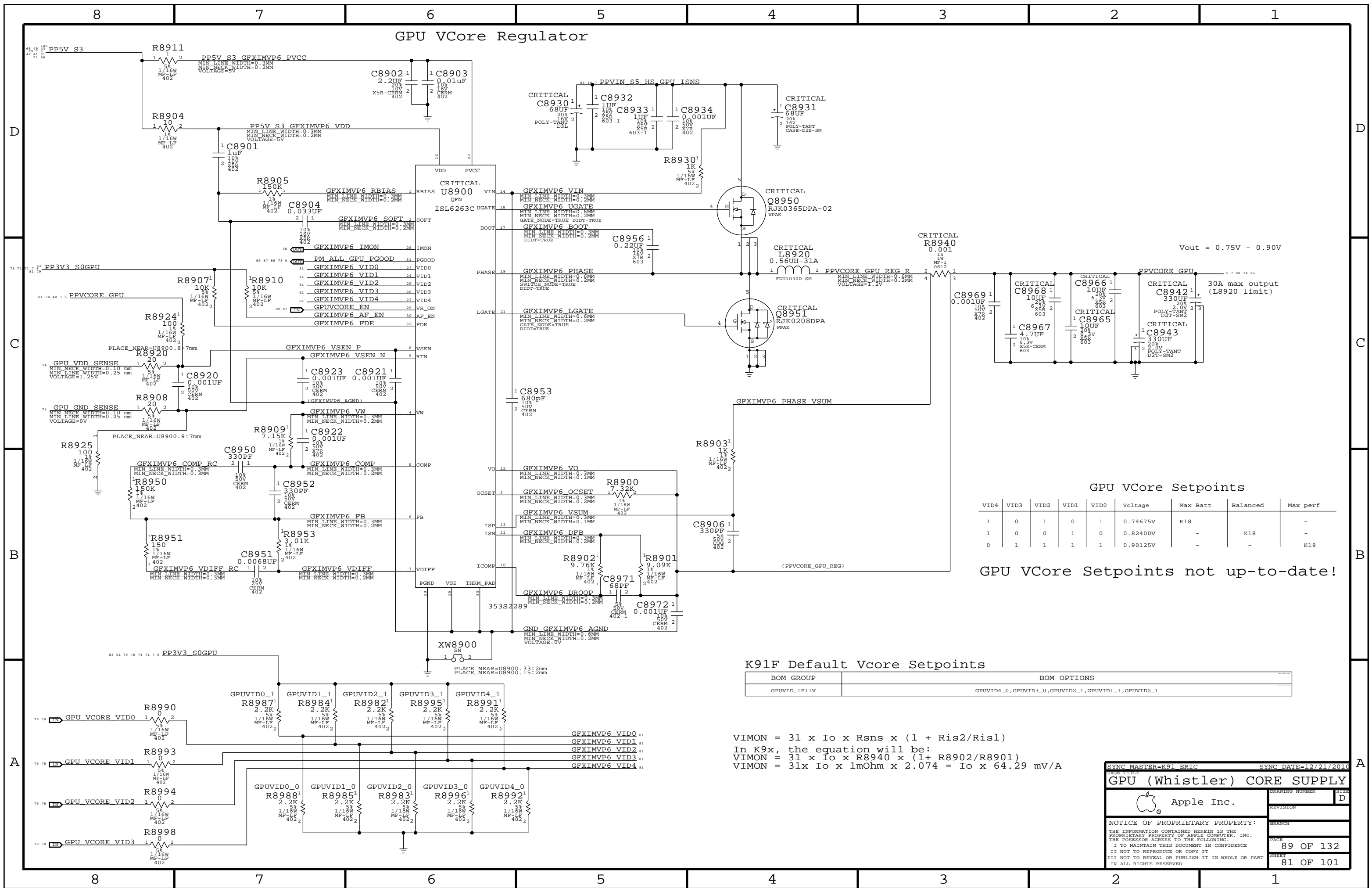
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VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

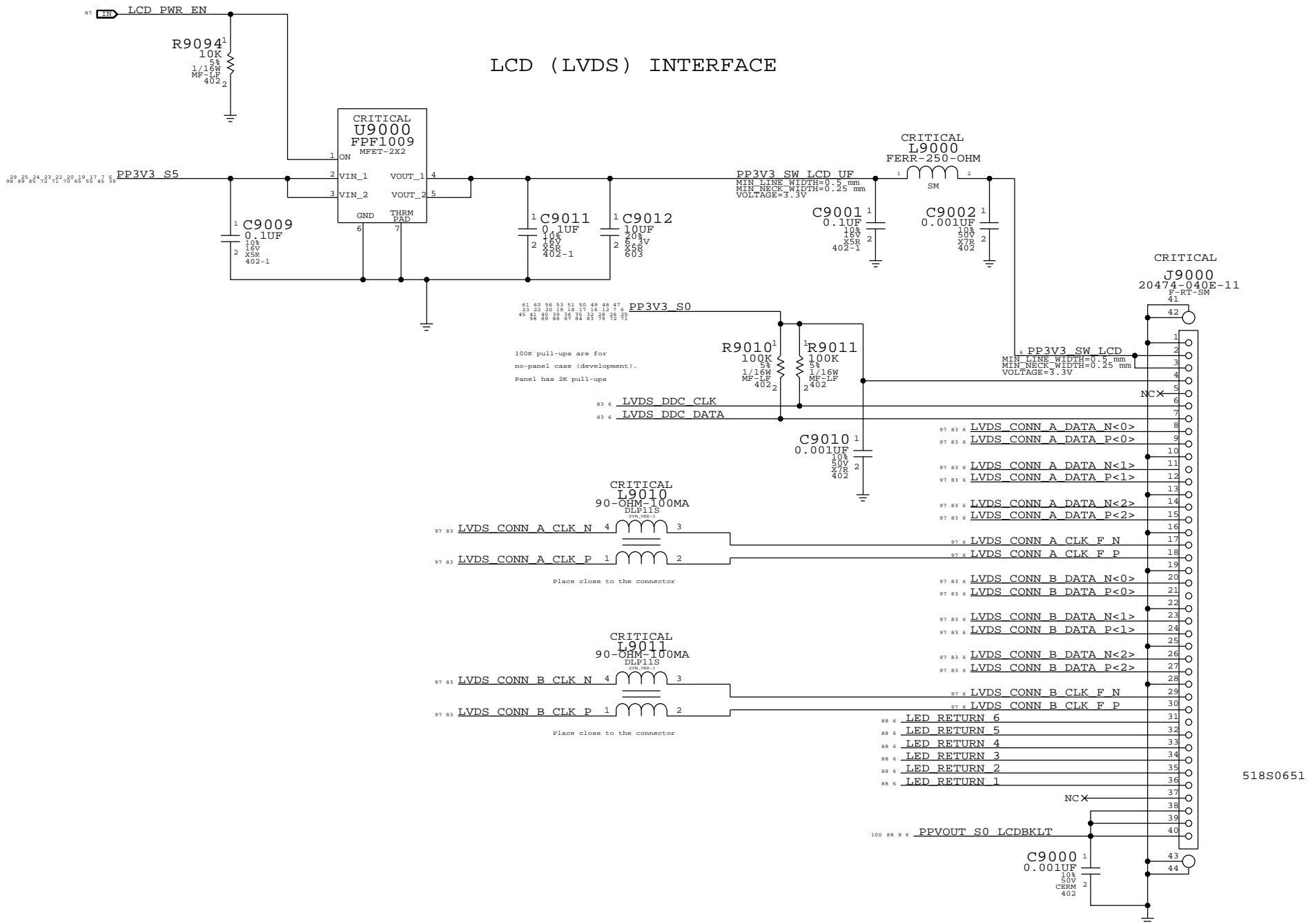
SYNCH MASTER-K91 ERIC		SYNCH DATE=12/21/2010	
PAGE TITLE			
GPU (Whistler)		CORE SUPPLY	
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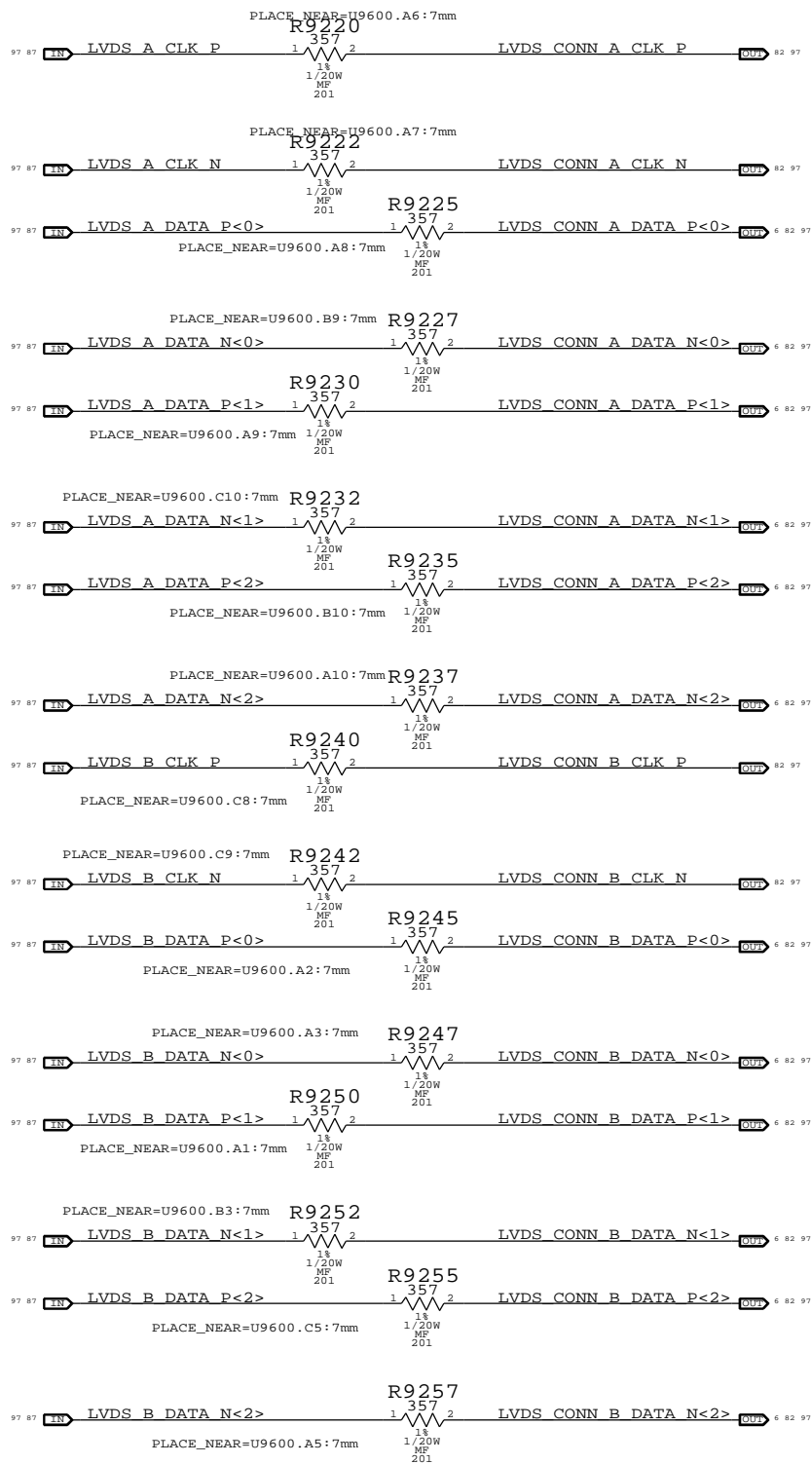
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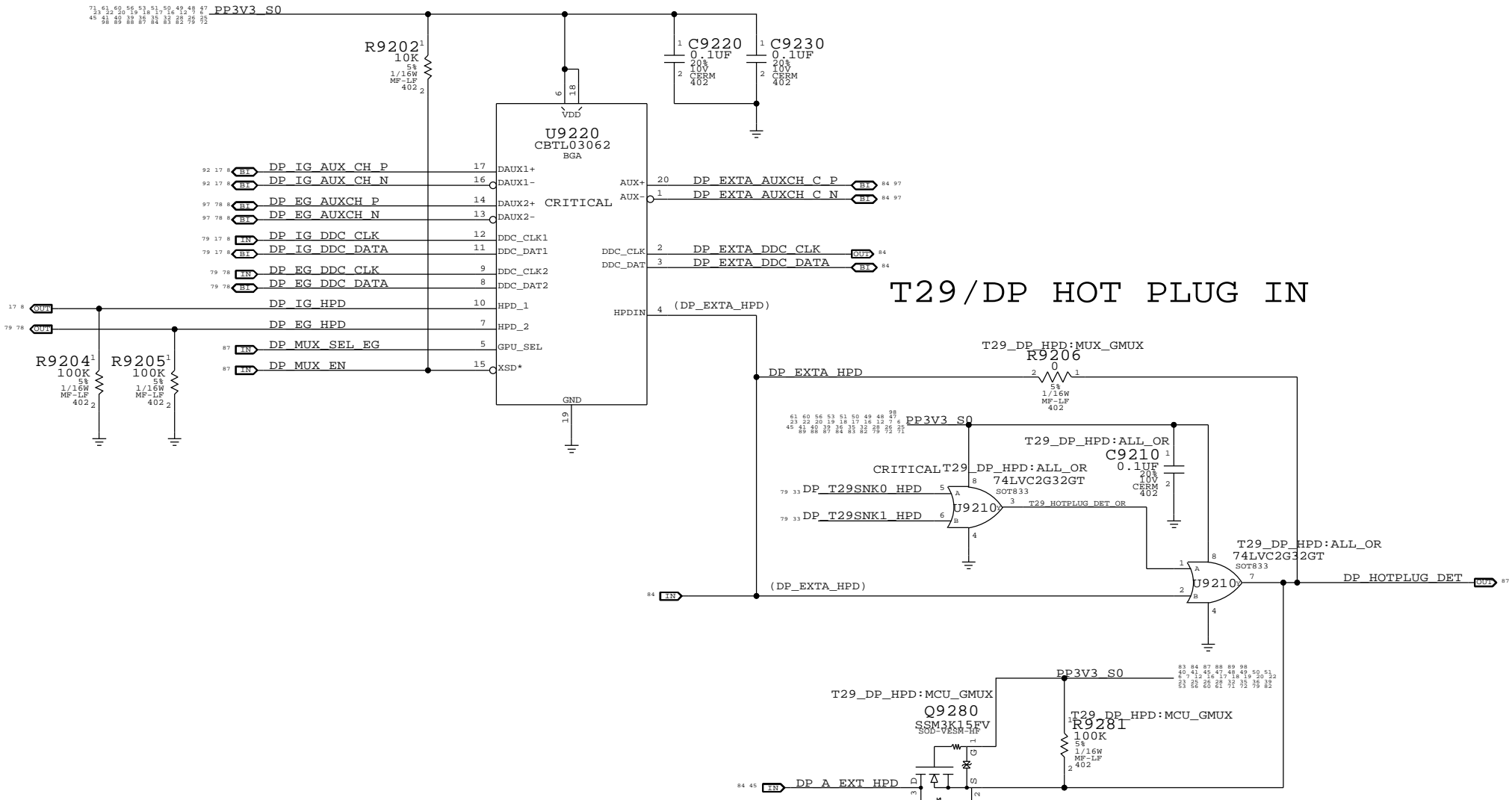
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LVDS Transmitter Termination

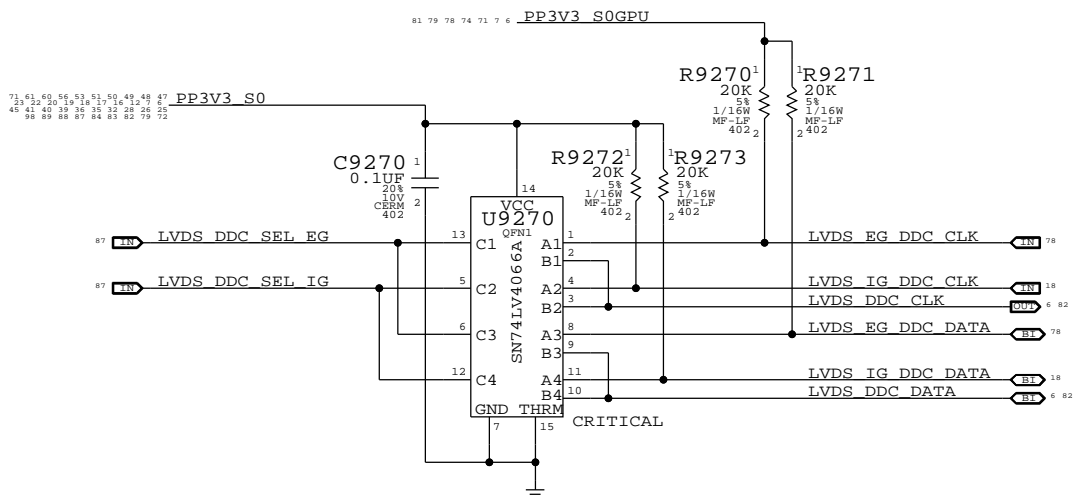
All emulated LVDS outputs require this termination



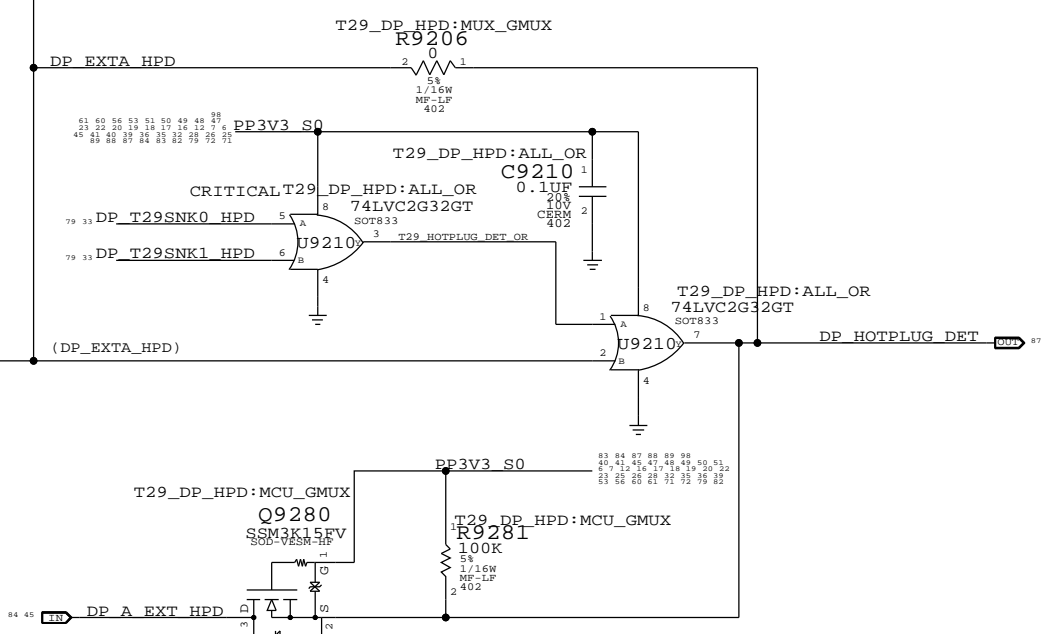
DP AUX, DDC, & HPD muxing to IG/EG



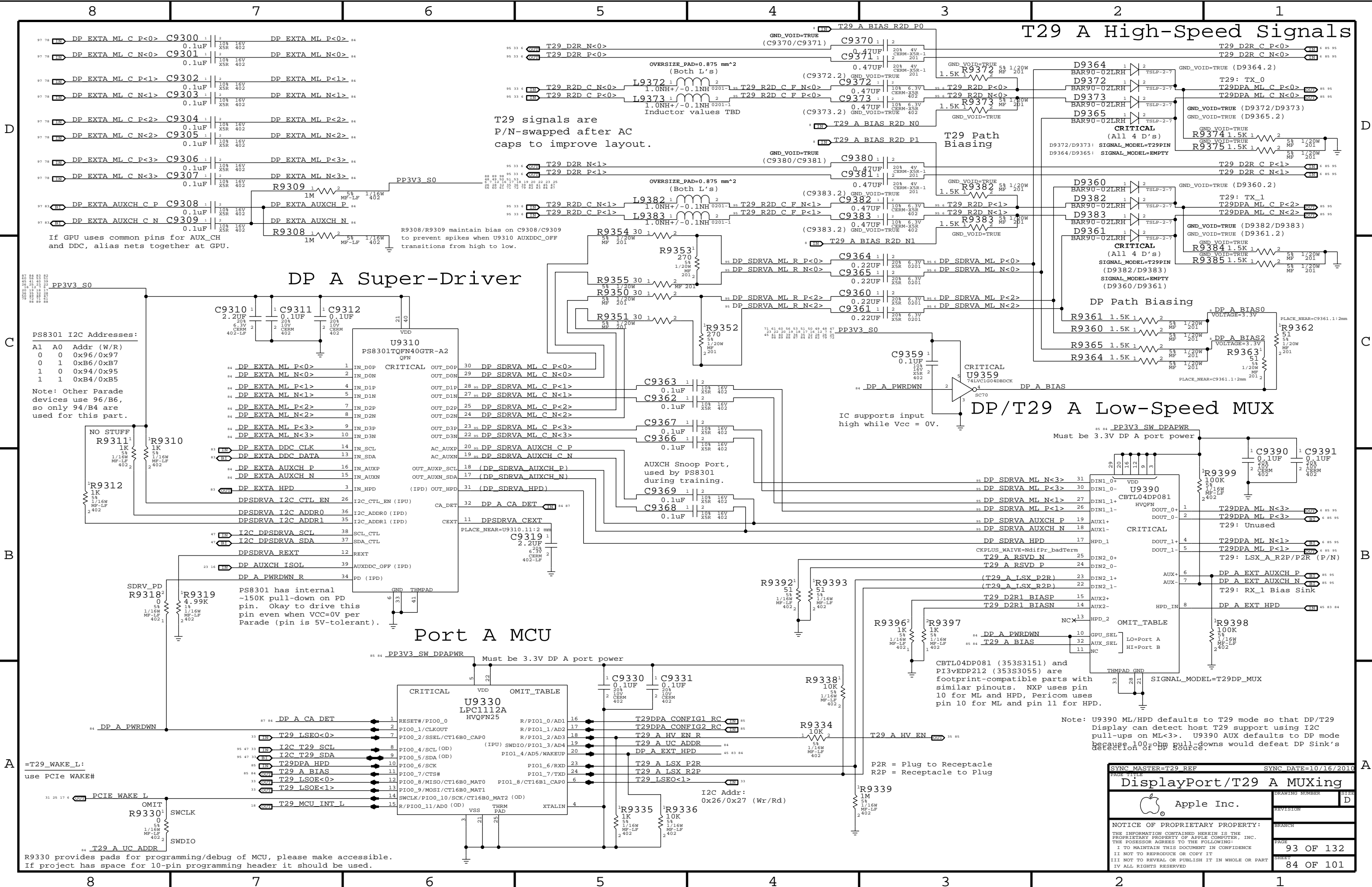
LVDS DDC MUX



T29/DP HOT PLUG IN



SYNC MASTER=K92 MLB		SYNC DATE=11/21/2010	
PAGE TITLE			
Muxed Graphics Support			
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T29 signals are P/N-swapped after AC caps to improve layout.

DP A Super-Driver

T29 A High-Speed Signals

DP/T29 A Low-Speed MUX

Port A MCU

PS8301 I2C Addresses:
A1 A0 Addr (W/R)
0 0 0x96/0x97
0 1 0xB6/0xB7
1 0 0x94/0x95
1 1 0xB4/0xB5
Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

=T29_WAKE_L:
use PCIE_WAKE#

R9330 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

IC supports input high while Vcc = 0V.

Must be 3.3V DP A port power

CBTL04DP081 (353S3151) and PI3VEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC MASTER=T29 REF

SYNC DATE=10/16/2010

DisplayPort/T29 A MUXing

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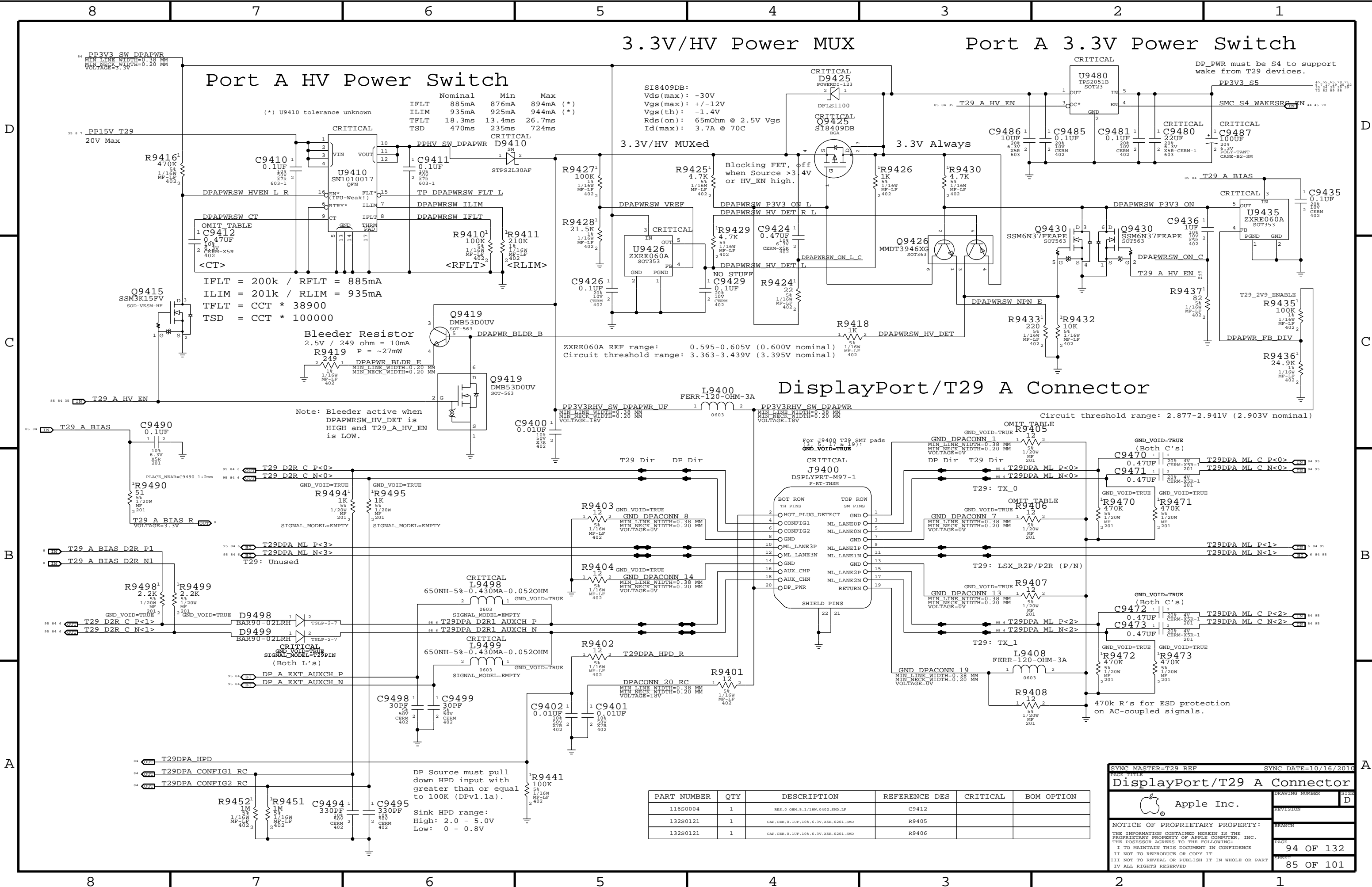
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Port A HV Power Switch

3.3V/HV Power MUX

Port A 3.3V Power Switch

DisplayPort/T29 A Connector

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES, 0 OHM, 5, 1/16W, 0402, SMD, LF	C9412		
132S0121	1	CAP, CER, 0.1UF, 10%, 6.3V, XSR, 0201, SMD	R9405		
132S0121	1	CAP, CER, 0.1UF, 10%, 6.3V, XSR, 0201, SMD	R9406		

SYNC MASTER=T29 REF

SYNC DATE=10/16/2010

DisplayPort/T29 A Connector

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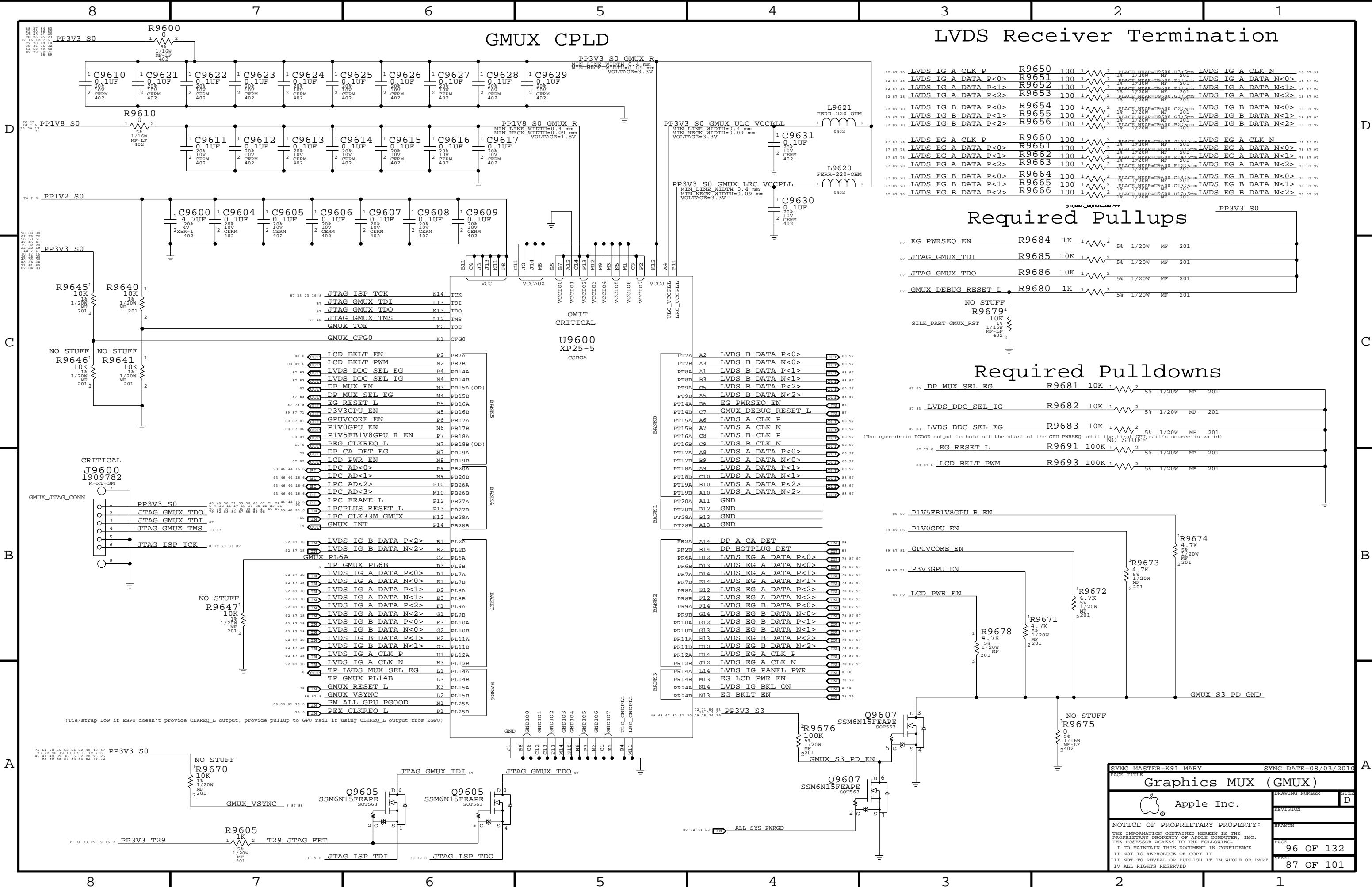
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LVDS Receiver Termination

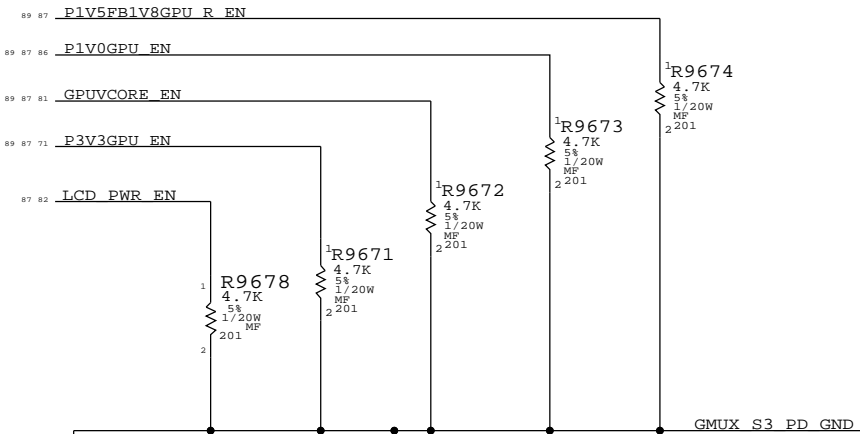
92 87 18	LVDS IG A CLK P	R9650	100	1	2	PLACE NEAR=U9600.H3:5mm	LVDS IG A CLK N	18 87 92
92 87 18	LVDS IG A DATA P<0>	R9651	100	1	2	PLACE NEAR=U9600.H1:5mm	LVDS IG A DATA N<0>	18 87 92
92 87 18	LVDS IG A DATA P<1>	R9652	100	1	2	PLACE NEAR=U9600.H3:5mm	LVDS IG A DATA N<1>	18 87 92
92 87 18	LVDS IG A DATA P<2>	R9653	100	1	2	PLACE NEAR=U9600.H1:5mm	LVDS IG A DATA N<2>	18 87 92
92 87 18	LVDS IG B DATA P<0>	R9654	100	1	2	PLACE NEAR=U9600.G2:5mm	LVDS IG B DATA N<0>	18 87 92
92 87 18	LVDS IG B DATA P<1>	R9655	100	1	2	PLACE NEAR=U9600.G3:5mm	LVDS IG B DATA N<1>	18 87 92
92 87 18	LVDS IG B DATA P<2>	R9656	100	1	2	PLACE NEAR=U9600.B2:5mm	LVDS IG B DATA N<2>	18 87 92
97 87 78	LVDS EG A CLK P	R9660	100	1	2	PLACE NEAR=U9600.H1:5mm	LVDS EG A CLK N	78 87 97
97 87 78	LVDS EG A DATA P<0>	R9661	100	1	2	PLACE NEAR=U9600.H3:5mm	LVDS EG A DATA N<0>	78 87 97
97 87 78	LVDS EG A DATA P<1>	R9662	100	1	2	PLACE NEAR=U9600.H1:5mm	LVDS EG A DATA N<1>	78 87 97
97 87 78	LVDS EG A DATA P<2>	R9663	100	1	2	PLACE NEAR=U9600.H2:5mm	LVDS EG A DATA N<2>	78 87 97
97 87 78	LVDS EG B DATA P<0>	R9664	100	1	2	PLACE NEAR=U9600.G3:5mm	LVDS EG B DATA N<0>	78 87 97
97 87 78	LVDS EG B DATA P<1>	R9665	100	1	2	PLACE NEAR=U9600.G1:5mm	LVDS EG B DATA N<1>	78 87 97
97 87 78	LVDS EG B DATA P<2>	R9666	100	1	2	PLACE NEAR=U9600.H1:5mm	LVDS EG B DATA N<2>	78 87 97

Required Pullups

87	EG_PWRSEQ_EN	R9684	1K	1	2	5% 1/20W MF 201
87	JTAG_GMUX_TDI	R9685	10K	1	2	5% 1/20W MF 201
87	JTAG_GMUX_TDO	R9686	10K	1	2	5% 1/20W MF 201
87	GMUX_DEBUG_RESET_L	R9680	1K	1	2	5% 1/20W MF 201

Required Pulldowns

87 83	DP_MUX_SEL_EG	R9681	10K	1	2	5% 1/20W MF 201
87 83	LVDS_DDC_SEL_IG	R9682	10K	1	2	5% 1/20W MF 201
87 83	LVDS_DDC_SEL_EG	R9683	10K	1	2	5% 1/20W MF 201
87 73 8	EG_RESET_L	R9691	100K	1	2	5% 1/20W MF 201
88 87 6	LCD_BKLT_PWM	R9693	100K	1	2	5% 1/20W MF 201



SYNC MASTER=K91 MARY

SYNC DATE=08/03/2010

Graphics MUX (GMUX)

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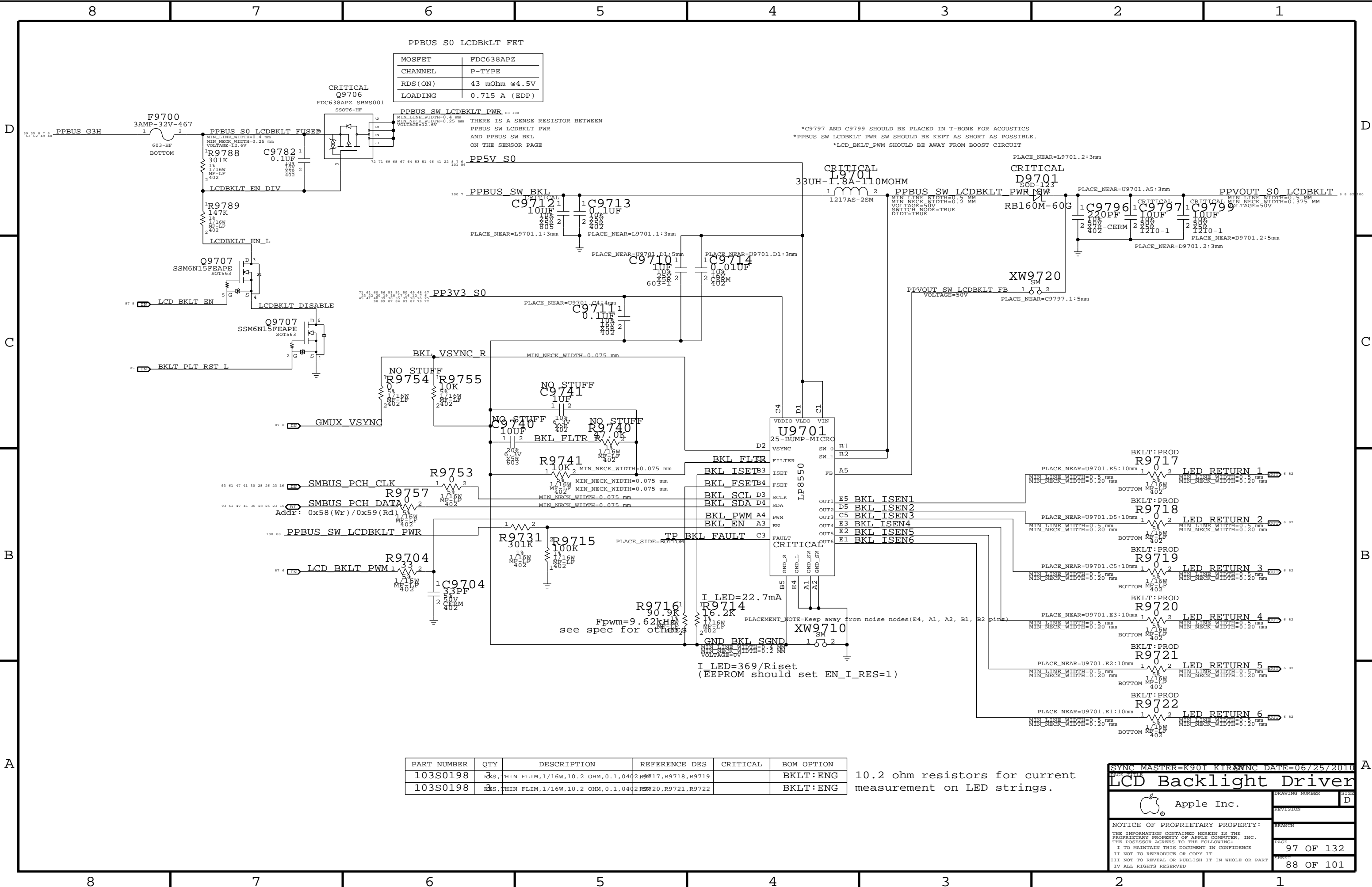
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	1	RES, THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0.0402	R9717, R9718, R9719		BKLT:ENG
103S0198	1	RES, THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0.0402	R9720, R9721, R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K901 KIRASVNC DATE=06/25/2010

LCD Backlight Driver

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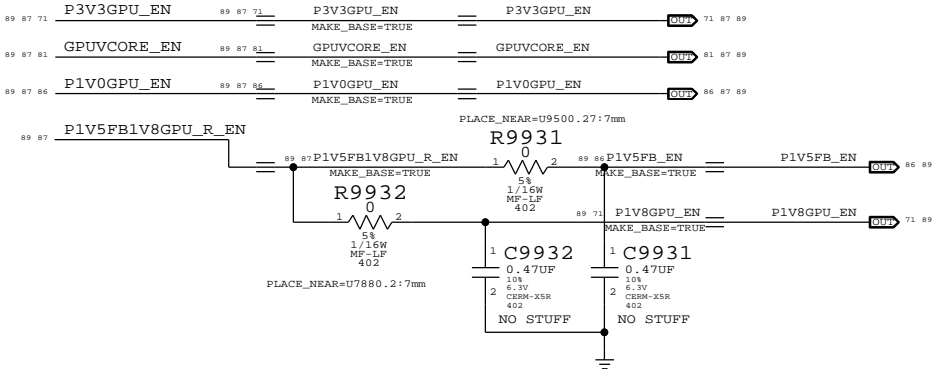
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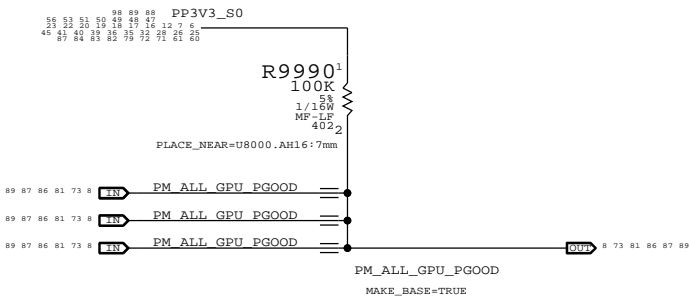
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GPU Rail Sequencing

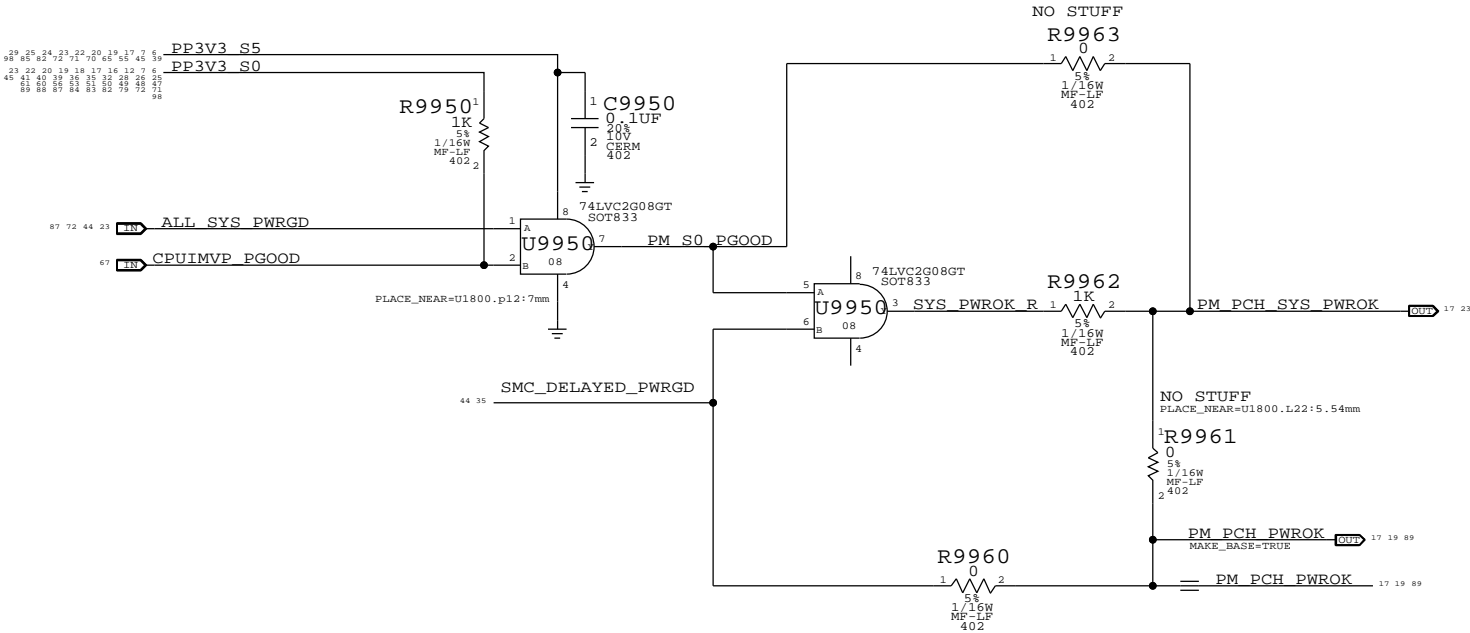
Whistler GPU requires rails to come up in the following order:
1) GPU_3.3V
2) GPUVcore
3) GPU_1.0V
4) GPU_1.8V/GDDR5 1.5/1.35V



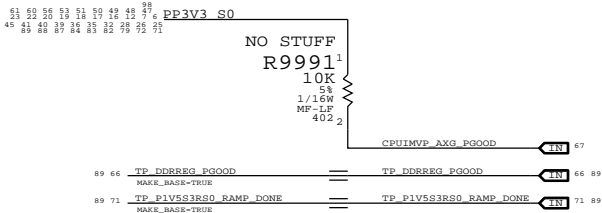
EXT GPU PWRGD Pullup




PCH S0 PWRGD



Unused PGOOD signal



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PAGE TITLE		Power Sequencing EG/PCH S0	
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87654321

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?


SPI Interface Constraints

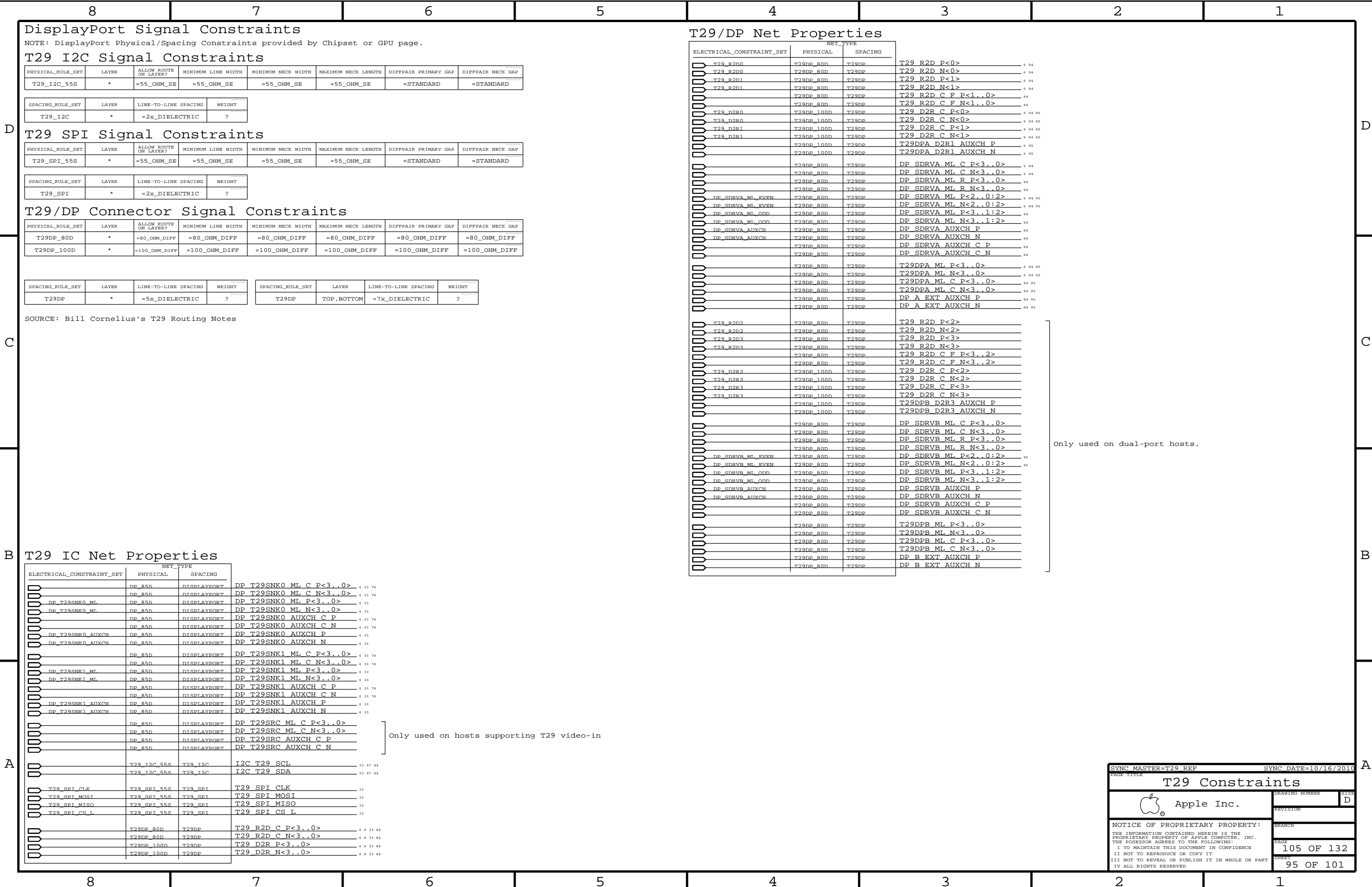
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties


ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL		SPACING	
	LPC_AD	LPC_50S	LPC	LPC_AD<3..0>		6	16 44 46 87
	LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L		6	16 44 46 87
	LPC_RESET_L	LPC_50S	LPC	LPCLPLUS RESET_L		6	25 46 87
	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R		18	25
		CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC		25	44
		CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCLPLUS		6	25 46
	SMBUS_PCH_CLK	SMR_50S	SMR	SMBUS_PCH_CLK		16	23 26 28 30 41 47 61 88
	SMBUS_PCH_DATA	SMR_50S	SMR	SMBUS_PCH_DATA		16	23 26 28 30 41 47 61 88
	SMBUS_PCH_0_CLK	SMR_50S	SMR	SML_PCH_0_CLK		16	47
	SMBUS_PCH_0_DATA	SMR_50S	SMR	SML_PCH_0_DATA		16	47
	SMBUS_PCH_1_CLK	SMR_50S	SMR	SML_PCH_1_CLK		16	47
	SMBUS_PCH_1_DATA	SMR_50S	SMR	SML_PCH_1_DATA		16	47
	HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK		16	56
		HDA_50S	HDA	HDA_BIT_CLK_R		16	
	HDA_SYNC	HDA_50S	HDA	HDA_SYNC		16	56
		HDA_50S	HDA	HDA_SYNC_R		16	
	HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L		16	
		HDA_50S	HDA	HDA_RST_L		16	56
	HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0		16	56
		HDA_50S	HDA	AUD_SDI_R		56	
	HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT		16	56
		HDA_50S	HDA	HDA_SDOUT_R		16	
	SPI_CLK	SPI_55S	SPI	SPI_CLK_R		16	46
		SPI_55S	SPI	SPI_CLK		46	
	SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R		16	46
		SPI_55S	SPI	SPI_MOSI		46	
	SPI_MISO	SPI_55S	SPI	SPI_MISO		16	46
	SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L		16	46
		SPI_55S	SPI	SPI_CS0_L		46	
		PCIE_85D	PCIE	PCIE_ENET_R2D_P		36	
		PCIE_85D	PCIE	PCIE_ENET_R2D_N		36	
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P		16	36
		PCIE_85D	PCIE	PCIE_ENET_R2D_C_N		16	36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P		16	36
		PCIE_85D	PCIE	PCIE_ENET_D2R_N		16	36
		PCIE_85D	PCIE	PCIE_ENET_D2R_C_P		36	
		PCIE_85D	PCIE	PCIE_ENET_D2R_C_N		36	
		PCIE_85D	PCIE	PCIE_AP_R2D_P		6	31
		PCIE_85D	PCIE	PCIE_AP_R2D_N		6	31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P		16	31
		PCIE_85D	PCIE	PCIE_AP_R2D_C_N		16	31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P		6	16 31
		PCIE_85D	PCIE	PCIE_AP_D2R_N		6	16 31
		PCIE_85D	PCIE	PCIE_FW_R2D_P		38	
		PCIE_85D	PCIE	PCIE_FW_R2D_N		38	
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P		16	38
		PCIE_85D	PCIE	PCIE_FW_R2D_C_N		16	38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P		16	38
		PCIE_85D	PCIE	PCIE_FW_D2R_N		16	38
		PCIE_85D	PCIE	PCIE_FW_D2R_C_P		38	
		PCIE_85D	PCIE	PCIE_FW_D2R_C_N		38	
REF0		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P		16	
REF0		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N		16	
REF0	PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P		16	33
REF0		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N		16	33
REF0		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P		16	
REF0		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N		16	
REF0		CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P		16	
REF0		CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N		16	
REF0		CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK		16	
REF0		CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN		16	25
	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P		16	73
		CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N		16	73
	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P		16	76
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N		16	76

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AA

SMBus Charger Net Properties

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.





















GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SIGNS	
	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK P 75 76
	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK N 75 76
	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK P 75 76
	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK N 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 A<8..0> 6 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 A<8..0> 6 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 ABI L 6 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 ABI L 6 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 RAS L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 RAS L 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CAS L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CAS L 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 WE L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 WE L 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CKE L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CKE L 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CS L 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CS L 75 76
	FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<0> 6 75 76
H330	FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<1> 6 75 76
H330	FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<2> 6 75 76
H330	FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<3> 6 75 76
H330	FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<0> 6 75 76
H330	FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<1> 6 75 76
H330	FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<2> 6 75 76
H330	FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<3> 6 75 76
H330	FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<0> 6 75 76
H330	FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<1> 6 75 76
H330	FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<2> 6 75 76
H330	FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<3> 6 75 76
H330	FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<0> 6 75 76
H330	FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<1> 6 75 76
H330	FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<2> 6 75 76
H330	FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<3> 6 75 76
	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<0> 6 75 76
	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<0> 6 75 76
	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<1> 6 75 76
	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<1> 6 75 76
	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<0> 6 75 76
	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<0> 6 75 76
	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<1> 6 75 76
	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<1> 6 75 76
	FB_A0_DO_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A0 DO<7..0> 6 75 76
	FB_A0_DO_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A0 DO<15..8> 6 75 76
	FB_A0_DO_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A0 DO<23..16> 6 75 76
	FB_A0_DO_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A0 DO<31..24> 6 75 76
	FB_A1_DO_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A1 DO<7..0> 6 75 76
	FB_A1_DO_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A1 DO<15..8> 6 75 76
	FB_A1_DO_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A1 DO<23..16> 6 75 76
	FB_A1_DO_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A1 DO<31..24> 6 75 76
	FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB RESET L 75 76 77

GDDR5 FB B Net Properties


ELECTRICAL_CONSTRAINT_SET		DET_TYPE			
		PHYSICAL	ISACING		
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK P	75 77
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK N	75 77
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK P	75 77
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK N	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 A<8..0>	6 75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 A<8..0>	6 75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 ABI L	6 75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 ABI L	6 75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 RAS L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 RAS L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 CAS L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 CAS L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 WE L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 WE L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 CKE L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 CKE L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 CS L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 CS L	75 77
	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<0>	6 75 77
H100	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<1>	6 75 77
H100	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<2>	6 75 77
H100	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<3>	6 75 77
H100	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<0>	6 75 77
H100	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<1>	6 75 77
H100	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<2>	6 75 77
H100	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<3>	6 75 77
H100	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<0>	6 75 77
H100	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<1>	6 75 77
H100	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<2>	6 75 77
H100	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<3>	6 75 77
H100	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<0>	6 75 77
H100	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<1>	6 75 77
H100	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<2>	6 75 77
H100	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<3>	6 75 77
H100	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<0>	6 75 77
H100	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<0>	6 75 77
H100	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<1>	6 75 77
H100	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<1>	6 75 77
H100	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<0>	6 75 77
H100	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<0>	6 75 77
H100	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<1>	6 75 77
H100	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<1>	6 75 77
H100	FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<7..0>	6 75 77
H100	FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<15..8>	6 75 77
H100	FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<23..16>	6 75 77
H100	FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<31..24>	6 75 77
H100	FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<7..0>	6 75 77
H100	FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<15..8>	6 75 77
H100	FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<23..16>	6 75 77
H100	FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<31..24>	6 75 77

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	LVDS_A_CLK	LVDS_R5D	LVDS	LVDS A_CLK P 83 87
	LVDS_A_CLK	LVDS_R5D	LVDS	LVDS A_CLK N 83 87
	LVDS_A_DATA	LVDS_R5D	LVDS	LVDS A DATA P<2..0> 83 87
	LVDS_A_DATA	LVDS_R5D	LVDS	LVDS A DATA N<2..0> 83 87
	LVDS_B_CLK	LVDS_R5D	LVDS	LVDS B_CLK P 83 87
	LVDS_B_CLK	LVDS_R5D	LVDS	LVDS B_CLK N 83 87
	LVDS_B_DATA	LVDS_R5D	LVDS	LVDS B DATA P<2..0> 83 87
	LVDS_B_DATA	LVDS_R5D	LVDS	LVDS B DATA N<2..0> 83 87
		LVDS_R5D	LVDS	LVDS CONN A_CLK F P 6 82
		LVDS_R5D	LVDS	LVDS CONN A_CLK F N 6 82
		LVDS_R5D	LVDS	LVDS CONN B_CLK F P 6 82
		LVDS_R5D	LVDS	LVDS CONN B_CLK F N 6 82
		LVDS_R5D	LVDS	LVDS CONN A_CLK P 82 83
		LVDS_R5D	LVDS	LVDS CONN A_CLK N 82 83
		LVDS_R5D	LVDS	LVDS CONN A DATA P<2..0> 6 82
		LVDS_R5D	LVDS	LVDS CONN A DATA N<2..0> 6 82
		LVDS_R5D	LVDS	LVDS CONN B_CLK P 82 83
		LVDS_R5D	LVDS	LVDS CONN B_CLK N 82 83
		LVDS_R5D	LVDS	LVDS CONN B DATA P<2..0> 6 82
		LVDS_R5D	LVDS	LVDS CONN B DATA N<2..0> 6 82

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE			
		PHYSICAL	SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M		78 79
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M		78 79
LVD5_EG_A_CLK	LVD5_85D	LVD5	LVD5 EG A CLK P		78 87
LVD5_EG_A_CLK	LVD5_85D	LVD5	LVD5 EG A CLK N		78 87
LVD5_EG_A_DATA	LVD5_85D	LVD5	LVD5 EG A DATA P<2..0>		78 87
LVD5_EG_A_DATA	LVD5_85D	LVD5	LVD5 EG A DATA N<2..0>		78 87
LVD5_EG_A_DATA3	LVD5_85D	LVD5	NC LVD5 EG A DATA P<3>		78 79
LVD5_EG_A_DATA3	LVD5_85D	LVD5	NC LVD5 EG A DATA N<3>		78 79
LVD5_EG_B_DATA	LVD5_85D	LVD5	LVD5 EG B DATA P<2..0>		78 87
LVD5_EG_B_DATA	LVD5_85D	LVD5	LVD5 EG B DATA N<2..0>		78 87
LVD5_EG_B_DATA3	LVD5_85D	LVD5	NC LVD5 EG B DATA P<3>		78 79
LVD5_EG_B_DATA3	LVD5_85D	LVD5	NC LVD5 EG B DATA N<3>		78 79
DP_MT	DP_85D	DISPLAYPORT	DP EXTA ML C P<3..0>		78 84
			DP EXTA ML C N<3..0>		78 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EXTA AUXCH C P		83 84
			DP EXTA AUXCH C N		83 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUXCH P		8 78 8
			DP EG AUXCH N		8 78 8

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I701_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_I701_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	= STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	+	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		ENET_10G0	ENETCONN	ENETCONN P<3...0>
		ENET_10G0	ENETCONN	ENETCONN N<3...0>
	SENSE DIFFPAIR	THERM 1701 558	THERM	CPUTHMSNS D2 P
	SENSE DIFFPAIR	THERM 1701 558	THERM	CPUTHMSNS D2 N
	SENSE DIFFPAIR	THERM 1701 558	THERM	CPU THERMD P
	SENSE DIFFPAIR	THERM 1701 558	THERM	CPU THERMD N
	SENSE DIFFPAIR	THERM 1701 558	THERM	GPU THMSNS D P
	SENSE DIFFPAIR	THERM 1701 558	THERM	GPU THMSNS D N
	SENSE DIFFPAIR	THERM 1701 558	THERM	GPU TDIODE P
	SENSE DIFFPAIR	THERM 1701 558	THERM	GPU TDIODE N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	VCCSA50 CS P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	VCCSA50 CS N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	VCCSAISNS R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	VCCSAISNS R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS 1V5 S3 R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS 1V5 S3 R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUVCCIOS0 CS P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUVCCIOS0 CS N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUVCCIOISNS R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUVCCIOISNS R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	GPUISENS N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	GPUISENS P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS 1V5 S3 N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS 1V5 S3 P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS AIRPORT N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS AIRPORT N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS AIRPORT P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS AIRPORT P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS AIRPORT R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS AIRPORT R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HDD N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HDD P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HDD R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HDD R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS LCDBLK1 N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS LCDBLK1 P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS ODD N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS ODD P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS ODD R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS ODD R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS PP1V0 SOGPU P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS PP1V0 SOGPU N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS PP1V0 SOGPU R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS PP1V0 SOGPU R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	PP1V8 SOGPU P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	PP1V8 SOGPU N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	PP1V8 SOGPU R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	PP1V8 SOGPU R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	PP1V5 SOGPU P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	PP1V5 SOGPU N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	PP1V5 SOGPU R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	PP1V5 SOGPU R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUIIMPV ISNS1G P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUIIMPV ISNS1G N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUIIMPV ISNS1G R P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUIIMPV ISNS1G R N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HS OTHER P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HS OTHER N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HS GPU P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HS GPU N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HS COMPUTING P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	ISNS HS COMPUTING N
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUIIMPV ISNS P
	SENSE DIFFPAIR	SENSE 1701 558	SENSE	CPUIIMPV ISNS N

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
PCIE CLK100M AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN P 6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN N 6 31
	1T01_DIEFFPAIR		CHGR CSI R P 63
	1T01_DIEFFPAIR		CHGR CSI R N 63
	1T01_DIEFFPAIR		CHGR CSO R P 49 63
	1T01_DIEFFPAIR		CHGR CSO R N 49 63
(USB_EXTA)	USB_R5D	USB	USB2 EXTA MUXED P 42
(USB_EXTA)	USB_R5D	USB	USB2 EXTA MUXED N 42
(USB_EXTA)	USB_R5D	USB	USB2 LT1 P 6 42
(USB_EXTA)	USB_R5D	USB	USB2 LT1 N 6 42
	USB_R5D	USB	CONN USB2 BT P 6
	USB_R5D	USB	CONN USB2 BT N 6
	USB_R5D	USB	USB LT2 P 6 42
	USB_R5D	USB	USB LT2 N 6 42
SSM2375L	AUDIO_DIEFFPAIR	AUDIO	SSM2375L P 59
SSM2375L	AUDIO_DIEFFPAIR	AUDIO	SSM2375L N 59
SSM2375R	AUDIO_DIEFFPAIR	AUDIO	SSM2375R P 59
SSM2375R	AUDIO_DIEFFPAIR	AUDIO	SSM2375R N 59
SSM2375S	AUDIO_DIEFFPAIR	AUDIO	SSM2375S P 59
SSM2375S	AUDIO_DIEFFPAIR	AUDIO	SSM2375S N 59
SPKRCONN	DIEFFPAIR	AUDIO	SPKRCONN L OUT P 6 59 60
	DIEFFPAIR	AUDIO	SPKRCONN L OUT N 6 59 60
SPKRCONN	DIEFFPAIR	AUDIO	SPKRCONN R OUT P 6 59 60
	DIEFFPAIR	AUDIO	SPKRCONN R OUT N 6 59 60
SPKRCONN	DIEFFPAIR	AUDIO	SPKRCONN S OUT P 6 59 60
	DIEFFPAIR	AUDIO	SPKRCONN S OUT N 6 59 60
	USB_R5D	USB	USB TPAD R P 52
	USB_R5D	USB	USB TPAD R N 52
	SB_POWER		PF3V3 S5 45 55 65 70 71 72 82 85 89
	SB_POWER		PF3V3 S0 48 49 50 51 53 56 60 61 71 72
	SB_POWER		PP1V5 S3RS0 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89
	GND		GND

	8	7	6	5	4	3	2	1	
	K91 Board-Specific Spacing & Physical Constraints								
	BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION	
	TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.5.1	
D	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM	
	STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM				
	55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM				
	50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	45_OHM_SE	TOP, BOTTOM	Y	0.13 MM	0.13 MM				
	45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM				
	40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	37_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.095 MM				
	37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
C	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM				
	27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.154 MM	0.154 MM	0.200 MM	0.200 MM	0.200 MM	
	72_OHM_DIFF	ISL2, ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM	
	72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM	
	80_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM	
	80_OHM_DIFF	TOP, BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM	
	85_OHM_DIFF	ISL2, ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM	
	85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM	
	90_OHM_DIFF	ISL2, ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM	
	90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM	
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM	
	100_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM	
	100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM	
A	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
	110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
	110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM	
	110_OHM_DIFF	ISL2, ISL11	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM	
	110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM	
	8	7	6	5	4	3	2	1	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM


NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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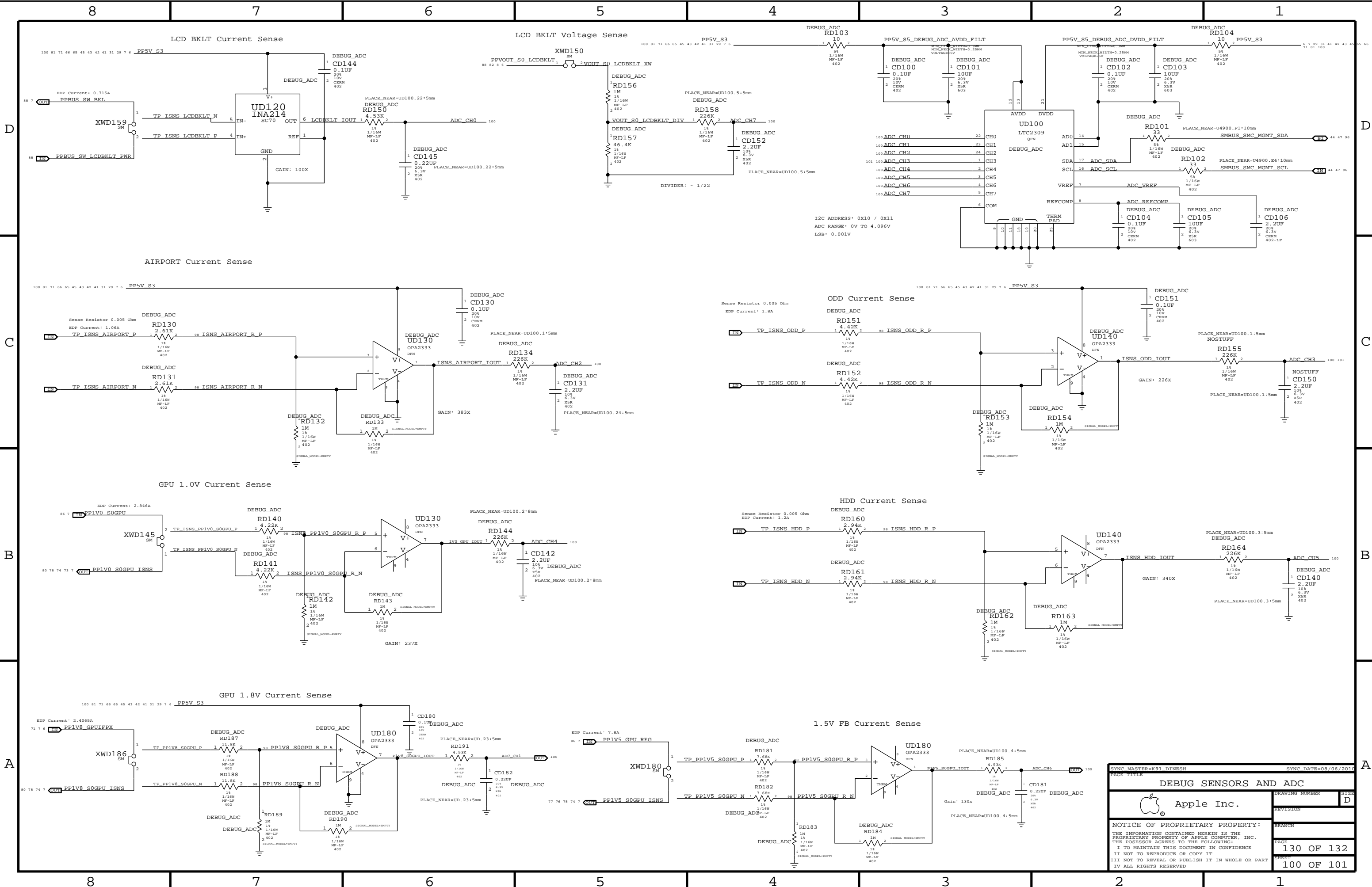
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